



SACRAMENTO
STATE

Course Change Proposal Form A



Academic Group (<i>College</i>): ECS	Academic Organization (<i>Department</i>): EEE	Date: 09/18/2006
Type of Course Proposal: New ___ Change <input checked="" type="checkbox"/> Deletion ___	Department Chair: Dr. Suresh Vadhva	Submitted by: Dr. Suresh Vadhva
Does this course fulfill a requirement for single-subject or multiple subject credential students? Yes ___ No <input checked="" type="checkbox"/>	For Catalog Copy: Yes <input checked="" type="checkbox"/> No ___ CCE: Yes ___ No <input checked="" type="checkbox"/>	Semester Effective: Fall ___ Spring <input checked="" type="checkbox"/> , 20_07__

This course replaces experimental course Subject Area (<i>prefix</i>) and Catalog Number (<i>course number</i>):	EEE 296K
This Catalog Number (<i>course number</i>) is being replaced:	

Change from:

Subject Area (<i>prefix</i>) & Catalog No. (<i>course no.</i>): EEE 296K	Title: Advanced VLSI Design	Units: 3
--	---------------------------------------	--------------------

Change to:

Subject Area (<i>prefix</i>) & Catalog No. (<i>course no.</i>): EEE 239	Title: Advanced VLSI Design-For-Test II	Units: 3
---	--	--------------------

JUSTIFICATION:

To build a greater knowledge depth among students of CMOS logic and VLSI fabrication, assembly and test operations. These are items that would make our students more competitive in the electronics industry.

NEW COURSE DESCRIPTION: (Not to exceed 80 words, and language should conform to catalog copy. See <http://www.csus.edu/acaf/univmanual/crspsl.htm> - Guidelines for Catalog Course Description)

Advanced topics in VLSI testing and Design-For-Test applications. Memory-specific test methodology and special features of memory designs employed in high volume manufacturing for improved testability, yield, and reliability. VLSI failure modes, their detection and prevention. Application of trim, redundancy, wear-leveling and error correction.

Note:	
Prerequisite: EEE 238	
Corequisite:	
CAN (California Articulation Number):	
Graded: Letter <input checked="" type="checkbox"/> Credit/No Credit ___	Instructor Approval Required? Yes ___ No <input checked="" type="checkbox"/>
Course Classification (<i>e.g., lecture, lab, seminar, discussion</i>): C5 Lecture	Title for SIS+/CMS (not more than 30 characters) Adv VLSI Design-For-Test II
Cross Listed? Yes ___ No <input checked="" type="checkbox"/>	If yes, do they meet together and fulfill the same requirement, and what is the other course.
How Many Times Can This Course be Taken for Credit? Once	
Can the course be taken for Credit more than once during the same term? Yes ___ No <input checked="" type="checkbox"/>	

FOR NEW COURSE PROPOSALS OR SUBSTANTIVE CHANGES ONLY:

Description of the Expected Learning Outcomes: Describe outcomes using the following format: "Students will be able to: 1), 2), etc." See the example at <http://www.csus.edu/acaf/example.htm>

Students will become familiar with the advanced issues involved with taking a finished integrated circuit design and developing it into a validated, mass production-worthy product. Students will learn the problems encountered in the development of integrated circuits and the methods used to solve them.

****Attach a list of the required/recommended course readings and activities [Note: it is understood that these are updated and modified as needed by the instructor(s).] This attachment should be forwarded only to your Dean's office, not Academic Affairs.**

Assessment Strategies: A description of the assessment strategies (e.g., portfolios, examinations, performances, pre-and post-tests, conferences with students, student papers) which will be used by the instructor to determine the extent to which students have achieved the learning outcomes noted above:

**Evaluations will be based on the following:
2 midterm exams and 1 final exam
Research term paper**

For whom is this course being developed?
 Majors in the Dept Majors of other Depts Minors in the Dept General Education Other
 Is this course required in a degree program (major, minor, graduate degree, certificate)? Yes No
 If yes, identify program(s): _____

 Does the proposed change or addition cause a significant increase in the use of College or University resources (lab room, computer facilities, faculty, etc.)? Yes No
 If yes, attach a description of resources needed and verify that resources are available.

 Indicate which department or programs will be affected by the proposed course (if any). _____

The Department Chair's signature below indicates that affected programs have been sent a copy of this proposal form.

Approvals: If proposed change, new course or deletion is approved, sign and date below. If not approved, forward without signing to the next reviewing authority, and attach an explanatory memorandum to the original copy.

Signatures:

	Date
Department Chair: <i>Scimita Valle</i>	11/21/2006
College Dean or Associate Dean: <i>[Signature]</i>	11/21/06
CPSP (for school personnel courses ONLY)	
Associate Vice President and Dean for Academic Programs	

Distribution: Academic Affairs (original), Department Chair and College Dean. Dean's office to send original after approval to Academic Affairs, at mail zip 6016. An electronic copy must also be sent.

New Course Offering: EEE 239

CLASS SYLLABUS

<u>Prerequisite</u>	This class follows EEE 238
<u>Instructor:</u>	Reed Linde, Product Engineering Manager, Flash Product Group, Intel Corporation
<u>Required Material:</u> Textbook TBD.	Instructor supplied material and industry references.
<u>Grading:</u>	Homework (15%), Midterm Exams (40%), Final Exam (25%), Research Paper or Project (TBD)(20%)

Course content and intent:

This course is supplemental to the topics covered in EEE 238, both in scope and in depth.

EEE 238 is a survey course, focused primarily on CMOS logic product manufacturing and development. It covers prototypical manufacturing flows for VLSI fab, assembly, and test operations as well as the key concerns related to product development and manufacturing cost, yield, and quality/reliability. Emphasis is on the common methods employed for the testing and DFT of IC logic products. This proposed follow-on course will build upon the content of EEE 238, going into greater depth on the topics of VLSI failure modes and their detection and prevention. The course will use the dominant VLSI industry memory technologies of SRAM, DRAM, and flash memory as vehicles to illustrate failure modes that impact product yield and quality/reliability, and will focus on the tools and methods used to detect, monitor, and systematically address these problems.

The focus on memory technology will also provide insight into VLSI test and DFT applications beyond what is covered in EEE 238, covering additionally memory-specific test methodology and special features of memory designs employed in high volume manufacturing for improved testability, yield, and reliability. Examples of such features include PBIST and DAT test modes, memory test patterns and methods for structural test, and the application of trims, redundancy, wear-leveling, and error correction.

Schedule

- Week 1 Review course syllabus. Overview of VLSI memory technologies and applications.
- Week 2 Flash memory overview – principles of operation, memory cell structure and physics, array and design architecture, and test methods/flows
- Week 3 Common intrinsic and extrinsic silicon failure modes of Flash memory. Examples and theory.
- Week 4 SRAM/cache memory overview – principles of operation, memory cell structure and physics, array and design architecture, and test methods/flows
- Week 5 Common intrinsic and extrinsic silicon failure modes SRAM/cache memory. Examples and theory.

Midterm 1

- Week 6 DRAM memory overview – principles of operation, memory cell structure and physics, array and design architecture, and test methods/flows
- Week 7 Common intrinsic and extrinsic silicon failure modes of DRAM. Examples and theory.
- Week 8 VLSI product validation methodologies and validation tools. Design validation and system validation methodologies. Simulation to silicon correlation. Product skew lot characterization.
- Week 9 Electrical failure analysis tools and techniques. Yield models and failure classification, analytical test and margin testing, memory raster and schmoo analysis, use of logic analyzer and digital oscilloscope.
- Week 10 Physical failure analysis tools and techniques. Circuit isolation (ion mill), circuit microprobing, emission microscopy, voltage contrast microscopy, stripback and staining, SEM and TEM microscopy.

Midterm 2

Week 11 Principles of IC reliability measurement and assessment. Origins of reliability specifications. Accelerated reliability assessment through silicon and package stresses. Arrhenius relationship.

Week 12 Q&R validation and manufacturing monitors. Product Q&R validation and qualification methodology. Customer-perceived Q&R. Statistical process control in IC manufacturing. Reliability statistics.

Week 13 Origins of design rules for memory technology yield and reliability manufacturing margin. Design and silicon process solutions for common CMOS technology issues.

Week 14 Design techniques for enhancing memory technology yield and reliability. Q&R applications of ATD. Application of trims. Memory array error correction, wear-leveling, and redundancy applications.

Week 15 Economics of VLSI memory technology yield and Q&R engineering

Finals