



SACRAMENTO
STATE

Course Change Proposal Form A



Academic Group (College): Engineering & Computer Science	Academic Organization (Department): Electrical & Electronic Engineering	Date: 9/16/2008
Type of Course Proposal: New <input checked="" type="checkbox"/> Change <input type="checkbox"/> Deletion <input type="checkbox"/>	Department Chair: Suresh Vadhva	Submitted by: Suresh Vadhva
Does this course fulfill a requirement for single-subject or multiple subject credential students? Yes <input type="checkbox"/> No <input checked="" type="checkbox"/>	For Catalog Copy: Yes <input checked="" type="checkbox"/> No <input type="checkbox"/> CCE: Yes <input type="checkbox"/> No <input checked="" type="checkbox"/>	Semester Effective: Fall <input type="checkbox"/> Spring <input checked="" type="checkbox"/> , 2009

This course replaces experimental course Subject Area (prefix) and Catalog Number (course number):	
This Catalog Number (course number) is being replaced:	

Change from:

Subject Area (prefix) & Catalog No. (course no.):	Title:	Units:
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Change to:

Subject Area (prefix) & Catalog No. (course no.): EEE 270	Title: Advanced Topics in Logic Design	Units: 4
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JUSTIFICATION:

This course is designed for EEE Graduate Students interested in digital design using Hardware Description Languages. A course is needed for them to learn and practice the techniques used to develop complex digital systems, as well as gain experience with typical computer-aided design (CAD) tools used for this purpose. This class will provide each student with the background and knowledge needed to design, synthesis and simulations digital circuits. Students will practice these skills through laboratory experiments and projects. The equipment and CAD software needed to support this class is already available in EEE.

NEW COURSE DESCRIPTION: (Not to exceed 80 words, and language should conform to catalog copy. See <http://www.csus.edu/acaf/univmanual/crspsl.htm> - Guidelines for Catalog Course Description)

Synchronous and asynchronous state machines. Timing issues in high-speed digital design. Design of a complex system using VHDL and Verilog Hardware Description Languages in a CAD environment. Automation toolsets to synthesize projects containing a hierarchy of modules into Field Programmable Gate Arrays (FPGAs). Simulations using CAD tools to verify the design before implementation on rapid prototyping boards in the lab. Lecture 3 hours; laboratory 3 hours.
Prerequisite: EEE Graduate Student Standing.

Note:	
Prerequisite: EEE Graduate Student Standing	
Corequisite:	
CAN (California Articulation Number):	
Graded: Letter <input checked="" type="checkbox"/> Credit/No Credit <input type="checkbox"/>	Instructor Approval Required? Yes <input type="checkbox"/> No <input checked="" type="checkbox"/>
Course Classification (e.g., lecture, lab, seminar, discussion): C4/16	Title for SIS+/CMS (not more than 30 characters) Adv Topics in Logic Design
Cross Listed? Yes <input type="checkbox"/> No <input checked="" type="checkbox"/>	If yes, do they meet together and fulfill the same requirement, and what is the other course.
How Many Times Can This Course be Taken for Credit? <u> 1 </u>	
Can the course be taken for Credit more than once during the same term? Yes <input type="checkbox"/> No <input checked="" type="checkbox"/>	

FOR NEW COURSE PROPOSALS OR SUBSTANTIVE CHANGES ONLY:

Description of the Expected Learning Outcomes: Describe outcomes using the following format: "Students will be able to: 1), 2), etc."
See the example at <http://www.csus.edu/acaf/example.htm>

Students will be able to design, simulate, analyze, implement and measure advanced logic circuits that include multiple, interlocked state machines. Specifically, students will design, simulate, analyze, implement and measure circuit for error detection and correction, CRC, scan chains, Analog to Digital Converter, synchronization, Displays, Keypads (typical consumer, home, industry, etc. applications). To simulate the circuits, students will learn to use high-level software design tools (HDLs).
Students will be able to compare and contrast the simulations and measurements during hands-on laboratory exercises

**Attach a list of the required/recommended course readings and activities [Note: it is understood that these are updated and modified as needed by the instructor(s).] This attachment should be forwarded only to your Dean's office, not Academic Affairs.

Assessment Strategies: A description of the assessment strategies (e.g., portfolios, examinations, performances, pre-and post-tests, conferences with students, student papers) which will be used by the instructor to determine the extent to which students have achieved the learning outcomes noted above:

The final exam on theory and design will be comprehensive.
Exam 1 – 20%
Exam 2 – 20%
Final – 20%
Projects & Reports – 20%
Laboratory – 20%

For whom is this course being developed?

Majors in the Dept Majors of other Depts ___ Minors in the Dept ___ General Education ___ Other ___

Is this course required in a degree program (major, minor, graduate degree, certificate)? Yes No ___

If yes, identify program(s): Computer Engineering

Does the proposed change or addition cause a significant increase in the use of College or University resources (lab room, computer facilities, faculty, etc.)? Yes ___ No

If yes, attach a description of resources needed and verify that resources are available.

Indicate which department or programs will be affected by the proposed course (if any). _____

The Department Chair's signature below indicates that affected programs have been sent a copy of this proposal form.

Approvals: If proposed change, new course or deletion is approved, sign and date below. If not approved, forward without signing to the next reviewing authority, and attach an explanatory memorandum to the original copy.

Signatures:

Date

Department Chair: <i>Suresh Yedhuru</i>	9/26/2008
College Dean or Associate Dean: <i>John Chelentz</i>	9/26/08
CPSP (for school personnel courses ONLY)	
Associate Vice President and Dean for Academic Programs	

Distribution: Academic Affairs (original), Department Chair and College Dean. Dean's office to send original after approval to Academic Affairs, at mail zip 6016. An electronic copy must also be sent.

EEE 270 Advanced Topics in Logic Design

Elective Course

Catalog Description: Synchronous and asynchronous state machines. Timing issues in high-speed digital design. Design of a complex system using VHDL and Verilog Hardware Description Languages in a CAD environment. Automation toolsets are used to synthesize projects containing a hierarchy of modules into Field Programmable Gate Arrays (FPGAs). Run simulations by using CAD tools to verify the design before implementation on rapid prototyping boards in the lab. **Prerequisite:** EEE Graduate Student Standing, 4 units.

Prerequisites: EEE Graduate Student Standing

Text: Smith, Douglas, HDL Chip Design, Doone Publications, 1996, ISBN 0-9651934-3-8,

Additional Support Material MAXplusII, HDL design package, Altera Corporation, Ver 10.0

Mano, M. Morris, Digital Design, Prentice Hall, 2002, ISBN 978-0-13-062121-4

Wakerly, John F., Digital Design: Principles and Practices, Prentice Hall, 2006, ISBN 978-0-13-173349-7

Course Objectives:

1. Provide in-depth design experiences that require students to:
 - a. develop good time management practices on their part
 - b. develop problem solving skills
 - c. meet design requirements and keep design within a resource limitation
 - d. think creatively on complex assignments
 - e. produce clear, concise written reports
 - f. learn how to associate with others in the course, yet do individual work
2. Cover wide-ranging topics in logic design at an advanced technical level
3. Students to become proficient in the use of high-level design tools including synthesis and simulation

Topics Covered:

1. State machine design: review of basics, self-clocking, algorithmic, interlocking state machines
2. VHDL: basics, simulation, synthesis to real hardware, test benches
3. FPGAs: architecture, implementation, configuration options, on-board memory, Altera or Xilinx examples
4. Testing: JTAG, boundary scan, chain scans, hazards in logic design, races, use of logic analyzers
6. Codes: error detection and correction schemes, CRC generation
7. Devices: ADC, LCDs, LCD drivers, memories, datapaths
8. Transmission line effect in logic design, active termination

Class Schedule:

Week	Topic	Text Pages
1	State machine review, self-clocking, Project #1 assigned	3-25, 195-201
2	VHDL basics	39-71
3	Altera FPGA, VHDL continued, metastability	Altera datasheet/web, 133-159
4	Keypad VHDL example, register/latch VHDL designs	163-173
5	LCD and LCD driver, timing control, Project #2 assigned	datasheet handout
6	VHDL synthesis, simulations, asynchronous inputs	201-217, 273-286
7	VHDL design techniques, test benches, hazards	75-110
8	Review and midterm exam	
9	JTAG, boundary scan, scan chains	handouts, Altera app. note
10	Verilog review, comparison to VHDL, project #3 assigned	re-read 133-217, 273-286
11	Codes, error detection and correction, CRC	handouts, 179-192
12	Review and midterm exam	
13	Memory, datapath control, bi-directional, ADC	handouts
14	Basic computer architecture, pipelining	refer to Mano text
15	Transmission line effect, active termination	refer to Wakerly text
16	Final exam	

Laboratory Schedule:

1. Project #1: VHDL (5 weeks) Build prototyping board, implement sequence detector, and decode keypad.
2. Project #2: VHDL (five weeks) Complex design with many interlocking state machines, precise timing control for I/O devices, memory interface, IP (Mega Wizards), resource limited, and with consumer appeal.
4. Project #3: Verilog (five weeks) Second complex design centered on data busses, dataflow and a RISC CPU.

Contribution of Course to Meeting the Professional Component:

1. ABET category content as estimated by faculty member who prepared this course description:
Engineering science: 0.5 units or 12.5 %, Engineering design: 3.5 units or 87.5 %
2. The far ranging, complex designs assigned as projects provide the student with real world engineering design experiences. Students learn from others, problem solve, learn how to minimize resources, and manage their time.

Course Outcomes:

- EEE 270 CO_1 Students will design systems based on logic that includes multiple, interlocked state machines
- EEE 270 CO_2 Students will understand 'synthesis' and technology when using high level design tools (HDLs)
- EEE 270 CO_3 Students will acquire extensive hands-on laboratory skills
- EEE 270 CO_4 Students will design implementations of error detection and correction, CRC, scan chains, ADC, synchronization, Displays, Keypads (typical consumer, home, industry, etc. applications)
- EEE 270 CO_5 Students will write a technical, grammatically correct report

Relationship of Course Outcomes to Program Outcomes: ABET designations, "a" through "k"

- a. ability to apply knowledge of mathematics, science, and engineering – EEE 270 CO_2 CO_4
Knowledge of electronics is required in the laboratory projects; students apply their knowledge of statistics when calculating mean time between failure, students use probability in one of their projects.
- b. an ability to design and conduct experiments, as well as to analyze and interpret data – EEE 270 CO_3
Logic analyzers collect signal data from actual hardware; students learn how to analyze and interpret what is, or is not, working properly – a major feature of this course.
- c. an ability to design a system, a component, or process to meet desired needs – EEE 270 CO_1 CO_4
The challenging projects have many design levels, requirements, and constraint limitations.
- d. an ability to function on multi-disciplinary teams – **Not applicable.**
- e. an ability to identify, formulate, and solve engineering problems – EEE 270 CO_1
Projects #2 and #3 force students to floorplan and formulate processes that lead to design solutions.
- f. an understanding of professional and ethical responsibility – EEE 270 CO_5
Students are constantly reminded that consulting with one another is professional and done in industry, however, copying solutions is not ethical and is not tolerated in this course; written assignments dealing with ethics are made.
- g. an ability to communicate effectively – EEE 270 CO_5
The reports from Projects #1 and #2 are graded critically by the instructors and often returned for re-writes; students are advised to keep either Project #2 or #3 for their EEE Career Portfolio.
- h. the broad education necessary to understand the impact of engineering solutions in a global and societal context – EEE 270 CO_4
Some of the projects over the years relate to common activities of our society (secrecy, security, games, identification, devices for homes, cars, etc).
- i. a recognition of the need for, and an ability to engage in life long learning – EEE 270 CO_2
Instructors describe new technology solutions for old problems, encourage students to read broadly, work "out of the box", and predict new technology that students should anticipate.
- j. a knowledge of contemporary issues - EEE 270 CO_4
Instructors include lecture material on issues such as security, safety, monitoring.
- k. an ability to use the techniques, skills, and modern engineering tools necessary for engineering practice – EEE 270 CO_2 CO_3
This course uses the most recent tools, equipment, and devices from industry (construction, testing, use of logic analyzers, universal programmers, download techniques).

Course Coordinator and Preparer of this Course Description: Professor Jing Pang

California State University, Sacramento
COLLEGE OF ENGINEERING AND COMPUTER SCIENCE

COURSE APPROVAL CHECKLIST

Please answer all questions (enter NA if not applicable)

1. Course number and title: EEE 270 – Advanced Topics in Logic Design
2. Old course number and:
3. Name of person in Charge: Dr. Suresh Vadhva
4. Is the course: ___ required X elective ___ service/GE
5. Check as appropriate: ___ change from 96/196/296
N/A change in description to reflect change in content
N/A change in prerequisite
N/A change in course format (e.g. lectures to lecture/lab)
N/A minor editing change in description
N/A change in number
N/A change in title
6. If offered as 96/196/296: ___ number of times ___ average enrollment
7. Does the proposed change or addition cause a significant increase in the use of School or University resources (lab room, computer facilities, faculty, etc.)? No. If yes, attach description of resources needed, including lab room number if appropriate, and verify that these resources are available.
8. For all changes (except change in number, title, or minor editing change in description) attach and check off here:
___ detailed syllabus ___ justification ___ old description
9. If there are related course changes, state numbers here and submit as a package
10. Date of department curriculum committee approval (if any) September 5, 2008.
11. Date of department faculty approval (if any) September 5, 2008.

FOR NEW COURSES (Including changes from 96/196/296)

Is the course related to or similar to any existing course? NO If so include explanation with justification.

Describe the target group of students.

This course is for EEE Graduate Students to use as an Elective in the Digital Area.

NOTE:

1. Syllabus should include title, author and date of text, name of instructor, main topics, amount or percentage of time devoted to each, description of special features such as term projects, and ABET or CSAB content category.
2. For required courses the justification must indicate how the new course fits into the overall curriculum and why changes are being made or the new course is being added.