



SACRAMENTO
STATE

Course Change Proposal Form A



Academic Group (College): Engineering & Computer Science	Academic Organization (Department): Computer Science Department	Date: November 12, 2008
Type of Course Proposal: New ___ Change <u>X</u> Deletion ___	Department Chair: Anne-Louise Radimsky	Submitted by: Anne-Louise Radimsky
Does this course fulfill a requirement for single-subject or multiple subject credential students? Yes ___ No <u>X</u>	For Catalog Copy: Yes <u>X</u> No ___ CCE (Extension): Yes ___ No <u>X</u>	Semester Effective: Fall <u>X</u> Spring __, 2009__

This course replaces experimental course Subject Area (prefix) and Catalog Nbr (course number):	
If changing an existing course, should new version be considered a repeat of the original version? If so, the same Course ID will be maintained. If not, a new Course ID will be assigned. Note: In PeopleSoft terminology, the Course ID is the unique system identifier, not the Catalog Nbr.	Yes <u>X</u> No ___

Change from:

Subject Area (prefix) & Catalog Nbr (course no.): CSC 242	Title: Computer-Aided Systems Design and Verification	Units: 3
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Change to:

Subject Area (prefix) & Catalog Nbr (course no.): N/A	Title: N/A	Units: N/A
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JUSTIFICATION:

Change in prerequisite only. Current Catalog Prerequisite is: CSC 205. The proposed New Catalog Prerequisite is: CSC 205 or CSC/EEE 273. The proposed change will allow well prepared EEE graduate students to enroll into CSC 242.

NEW COURSE DESCRIPTION: (Not to exceed 80 words, and language should conform to catalog copy. See <http://www.csus.edu/umannual/acad.htm> - Guidelines for Catalog Course Description)

N/A

Note:

Prerequisite: Proposed new prerequisite: CSC 205 OR CSC/EEE273	
Enforced at Registration: Yes <u>X</u> No ___	
Corequisite:	
Enforced at Registration: Yes ___ No ___	
Graded: Letter <u>X</u> Credit/No Credit ___	Instructor Approval Required? Yes ___ No <u>X</u>
Course Classification (e.g., lecture, lab, seminar, discussion): Seminar	Title for CMS (not more than 30 characters) Compnr-Aided Sys Dsgn+Verifctn
Cross Listed? Yes ___ No <u>X</u>	If yes, do they meet together and fulfill the same requirement, and what is the other course.
How Many Times Can This Course be Taken for Credit? <u>1</u>	
Can the course be taken for Credit more than once during the same term? Yes ___ No <u>X</u>	

FOR NEW COURSE PROPOSALS OR SUBSTANTIVE CHANGES ONLY:

Description of the Expected Learning Outcomes: Describe outcomes using the following format: "Students will be able to: 1), 2), etc."
See the example at <http://www.csus.edu/acaf/example.htm>

****Attach a list of the required/recommended course readings and activities [Note: it is understood that these are updated and modified as needed by the instructor(s).] This attachment should be forwarded only to your Dean's office, not Academic Affairs.**

Assessment Strategies: A description of the assessment strategies (e.g., portfolios, examinations, performances, pre-and post-tests, conferences with students, student papers) which will be used by the instructor to determine the extent to which students have achieved the learning outcomes noted above:

For whom is this course being developed?

Majors in the Dept ___ Majors of other Depts ___ Minors in the Dept ___ General Education ___ Other ___

Is this course required in a degree program (major, minor, graduate degree, certificate)? Yes ___ No ___

If yes, identify program(s):

Does the proposed change or addition cause a significant increase in the use of College or University resources (lab room, computer facilities, faculty, etc.)? Yes ___ No ___

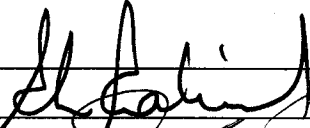
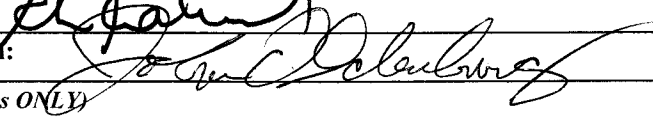
If yes, attach a description of resources needed and verify that resources are available.

Indicate which department or programs will be affected by the proposed course (if any). _____

The Department Chair's signature below indicates that affected programs have been sent a copy of this proposal form.

Approvals: If proposed change, new course or deletion is approved, sign and date below. If not approved, forward without signing to the next reviewing authority, and attach an explanatory memorandum to the original copy.

Signatures:

	Date
Department Chair: 	12/9/08
College Dean or Associate Dean: 	12/9/08
CPSP (for school personnel courses ONLY)	
Associate Vice President and Dean for Academic Programs	

Distribution: Academic Affairs (original), Department Chair and College Dean. Dean's office to send original after approval to Academic Affairs, at mail zip 6016. An electronic copy must also be sent.

California State University, Sacramento
College of Engineering and Computer Science
Department of Computer Science/ Computer Engineering Program

CSc 242
Computer-Aided Systems Design and Verification Fall 2008

Instructor: **Dr. Behnam S. Arad**
Professor of Computer Science
Office Hours*: Tuesday 3 – 4 pm; Thursday 2 – 4 pm
**changes to office hours will be announced on my web site*

Office: RVR 5044
Phone: (916) 278-7160
E-mail Address: arad@csus.edu

Course Description:

Design and verification methodology using hardware description and verification languages (HDVLS); Topics include: advances in IC chip design; introduction to HDVLS such as SystemVerilog; HDVL language basics including data types, arrays, structures, unions, procedural blocks, tasks, functions, and interface concept; design hierarchy; verification planning and productivity; verification infrastructure; guidelines for efficient verification of large designs; assertion-based verification; comprehensive computer-related design projects. Prerequisite: CSc 205; 3 units

Textbooks:

1. SystemVerilog for Design by Stuart Sutherland, Simon Davidmann, and Peter Flake, 2nd Edition Springer 2006
2. SystemVerilog for Verification by Chris Spear, Springer, 2nd Edition, Springer

Grading Policy:

Term Project and other Graded Assignments	30 %
Midterm	35%
Final Exam	35%

You may be required to submit a project report during the last week of school. Some Project presentations may be scheduled during the last week of classes.

Prerequisite: Prerequisite: CSc 205.

Policies:

1. Class attendance is expected. Prior to each exam, review guidelines will be provided. No make-up exam will be arranged unless there is a serious and compelling reason. The instructor must be notified prior to the exam, otherwise no make up will be given.

2. Graded Assignments are due at the beginning of the class on the due date. Each assignment should have a typed cover including the following information: Course number, Section, instructor, assignment number, due date, date submitted, and your name. You will also be asked to submit your code and test files electronically to the grader. Unless otherwise noted, late assignments submitted within one week from the due date will receive a %5 deduction. Late assignments will not be accepted once the solution has been posted. You must mark the assignment late.
3. All assignments and projects must be your independent work. All instances of academic dishonesty will be dealt with according to the CSUS academic honesty, policy & procedures. The minimum sanction for

each incident is that no credit will be issued to all students involved for the assignment/project. The university policy is posted at <http://www.csus.edu/admbus/manual/UMA00150.htm>

4. You can use a laptop during the lecture only if it is used to take notes to view lecture slides for this course. You should not use the system for other purposes during the lecture or in a manner that will disturb other students. All cell phones, pagers, and similar devices should be on a silent mode.
5. A web page has been created for the course to provide you with important course information in format and links to several useful sites. The page can be accessed from <http://gaia.ecs.csus.edu/~arad>. This web page is only for the students taking the course for credit. You must not share the access code with others.
6. This course involves working with several UNIX based EDA tools. You will be provided login and access code for using the tool on a Unix server. If you are not familiar with UNIX basic commands, you need to familiarize yourself during the first week of school. The access to the EDA tools is only for the students taking the course for credit. You must not provide access to others.
7. A mailing list has been set up for this course, **csc242**, to be used only by the instructor to send assignments, projects, and other important information to the students. Subscription to this list is required. To subscribe to this list electronically you need to send the following email message in text format from a CSUS account to majordomo@hera.csus.edu :

subject: leave blank
Message body: subscribe csc242
 end

Csc242 Tentative Course Outline*

Major Topics	hour(s)	References
Introduction	1	Course Outline
Overview of IC chip design process	1	lecture notes
Review of design using hardware description languages	3	lecture notes
Introduction to System Verilog	1	Sutherland Chapter 1 Spear Chapter 1
System Verilog basics including data types, structures, unions, and arrays	7	Sutherland Chapter 2 – 5 Spear Chapter 2
Procedural blocks & Statements	2	Sutherland Chapter 6-7 Spear Chapter 3
Interface concept and its application	6	Sutherland Chapter 10
Design Hierarchy	2	Spear Chapters 5, 9
Inter-process communication in SystemVerilog	2	Spear Chapter 7
Object oriented approach in verification	5	Spear Chapter 4
Verification methodology using SystemVerilog	6	Spear Chapter 5, 6, 9
Case studies involving computer design	3	
Exams and Review	2	

This is a tentative list of topics. Time permitting, other topics will be covered as well. In most cases more than one reference is provided to help you use different sources. Not all references given for each topic. Use your lecture notes as the main reference. Other references will be provided during the lecture if necessary.

CSC 242

JUSTIFICATION:

The proposed change will allow well prepared EEE graduate students to enroll into CSC 242.

OLD DESCRIPTION:

PLEASE NOTE: DESCRIPTION WILL NOT CHANGE.

Design and verification methodology using hardware description and verification languages (HDVLS). Advances in IC chip design; introduction to HDVLS such as System Verilog; HDVL language basics including data types, arrays, structures, unions, procedural blocks, tasks, functions, and interface concepts; design hierarchy; verification planning and productivity; verification infrastructure; guidelines for efficient verification of large designs; assertion-based verification; comprehensive computer-related design projects.