## Course Change Proposal
### Form A

**Academic Group (College):** ECS  
**Academic Organization (Department):** Computer Engineering Program  
**Date:** April 14, 2010  
**Submitted by:** Du Zhang

<table>
<thead>
<tr>
<th>Type of Course Proposal:</th>
<th>Department Chair: Suresh Vadhva</th>
<th>Semester Effective:</th>
</tr>
</thead>
<tbody>
<tr>
<td>New _ Change _ Deletion _</td>
<td></td>
<td>Fall _ Spring <strong>, 2010</strong></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Does this course fulfill a requirement for single-subject or multiple subject credential students?</th>
<th>For Catalog Copy:</th>
<th>CCE (Extension):</th>
</tr>
</thead>
<tbody>
<tr>
<td>Yes _ No _ X_</td>
<td>Yes <em>X</em> No _</td>
<td>Yes _ No _ X_</td>
</tr>
</tbody>
</table>

This course replaces experimental course **Subject Area (prefix) and Catalog Nbr (course number):**

If changing an existing course, should new version be considered a repeat of the original version? If so, the same Course ID will be maintained. If not, a new Course ID will be assigned. Note: In PeopleSoft terminology, the Course ID is the unique system identifier, not the Catalog Nbr.

<table>
<thead>
<tr>
<th>Subject Area (prefix) &amp; Catalog Nbr (course no.):</th>
<th>Title: Advanced Computer Organization</th>
<th>Units: 3.0</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPE 142</td>
<td></td>
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</table>

<table>
<thead>
<tr>
<th>Change to:</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Subject Area (prefix) &amp; Catalog Nbr (course no.):</strong></td>
</tr>
<tr>
<td>Same</td>
</tr>
</tbody>
</table>

### JUSTIFICATION:

The CPE 142 course content has changed to cover the latest computer architecture concepts and techniques including more coverage on parallel processing and use of EDA tools in modeling and verification of computer systems. The prerequisite has been changed to accommodate both CSC and CPE students.

Current Catalog Description: Design and performance issues of computers: CPU, I/O interface, and memory. Design alternatives for arithmetic functions, CPU internal architecture, instruction set, instruction cycle, I/O, interrupt, direct memory access, and bus and memory hierarchy. CAD tools for schematic capture and simulations. Students will design and simulate a microcomputer. Prerequisite: CSC 137 or equivalent. Cross-listed: CPE 142; only one may be counted for credit.

**NEW COURSE DESCRIPTION:** (Not to exceed 80 words, and language should conform to catalog copy. See http://www.csus.edu/umanual/acad.htm - Guidelines for Catalog Course Description)

Design and performance issues of computers. Instruction set architecture, computer arithmetic, processor design, survey of contemporary architectures, interfacing I/O devices, hierarchical memory design and analysis, parallelism and multiprocessor systems, techniques for enhancing performance, and an introduction to EDA tools for design and verification of computers. Design and simulation of a microcomputer in an HDL. Cross-listed as CSC 142.

**Note:** Open to students with full CSC or CPE major standing only.

**Prerequisite:** CSC 137 OR CPE 166 and CPE 185.

<table>
<thead>
<tr>
<th>Enforced at Registration:</th>
<th>Yes _ No _ X_</th>
</tr>
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</table>

**Corequisite:**

<table>
<thead>
<tr>
<th>Enforced at Registration:</th>
<th>Yes _ No _</th>
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</table>

Graded: Letter _X_ Credit/No Credit  
**Instructor Approval Required?** Yes _ No _ X_  
**Course Classification (e.g., lecture, lab, seminar, discussion):** Lecture  
**Title for CMS (not more than 30 characters):** Advanced Computer Organization

<table>
<thead>
<tr>
<th>Cross Listed?</th>
<th>If yes, do they meet together and fulfill the same requirement, and what is the other course.</th>
<th>Yes - CSC 142</th>
</tr>
</thead>
<tbody>
<tr>
<td>Yes <em>X</em> No _</td>
<td></td>
<td></td>
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</tbody>
</table>

**How Many Times Can This Course be Taken for Credit?** 1

**Can the course be taken for Credit more than once during the same term?** Yes _ No _ X_
FOR NEW COURSE PROPOSALS OR SUBSTANTIVE CHANGES ONLY:

Description of the Expected Learning Outcomes: Describe outcomes using the following format: “Students will be able to: 1), 2), etc.” See the example at http://www.csus.edu/aсаl/example.htm

- Students will be able to demonstrate a thorough understanding of:
  - Instruction pipelining
  - Processor design
  - Memory hierarchy and optimization
  - Basic understanding of:
    - Instruction set architecture
    - Integer and floating point arithmetic
    - Branch prediction and speculative execution
    - Super scalar and super pipelined instruction datapath
    - Improving memory bandwidth (memory architecture)
    - Improving data transfer rate (bus architecture)
    - Performance evaluation

- Students will also have exposure to:
  - The role of compiler optimization in enhancing performance
  - Data coherency in multiprocessor systems
  - Introduction to parallel architectures
  - Introduction to instruction-level parallelism
  - Introduction to distributed systems
  - EDA tools for design and simulation of computers

**Attach a list of the required/recommended course readings and activities [Note: it is understood that these are updated and modified as needed by the instructor(s).] This attachment should be forwarded only to your Dean’s office, not Academic Affairs.

Assessment Strategies: A description of the assessment strategies (e.g., portfolios, examinations, performances, pre-and post-tests, conferences with students, student papers) which will be used by the instructor to determine the extent to which students have achieved the learning outcomes noted above:

Technical reports and laboratory projects which include:
1. Introduction to Synopsys VCS Verilog Simulator (1 week)
2. Design and simulation of hardware components using Verilog HDL (3-4 weeks)
3. Students will design and simulate a microcomputer using Verilog HDL as part of the term project (5-6 weeks)

For whom is this course being developed?
- Majors in the Dept ___ Majors of other Depts ___ Minors in the Dept ___ General Education ___ Other ___

- Is this course required in a degree program (major, minor, graduate degree, certificate)? Yes ___ No ___

- If yes, identify program(s): Elective for CSC BS degree, required course for CPE BS degree.

Does the proposed change or addition cause a significant increase in the use of College or University resources (lab room, computer facilities, faculty, etc.)? Yes ___ No ___

- If yes, attach a description of resources needed and verify that resources are available.

- Indicate which department or programs will be affected by the proposed course. Computer Science

The Department Chair’s signature below indicates that affected programs have been sent a copy of this proposal form.

Approvals: If proposed change, new course or deletion is approved, sign and date below. If not approved, forward without signing to the next reviewing authority, and attach an explanatory memorandum to the original copy.

Signatures: Date

| Department Chair: | 4/23/2010 |
| College Dean or Associate Dean: | 4/23/10 |
| CPSP (for school personnel courses ONLY): | |
| Associate Vice President and Dean for Academic Programs: | |

Distribution: Academic Affairs (original), Department Chair and College Dean. Dean’s office to send original after approval to Academic Affairs, at mail zip 6016. An electronic copy must also be sent.
COURSE DESCRIPTION

Dept., Number  CPE 142  Course Title  Advanced Computer Organization
Semester hours  3  Course Coordinator  Behnam S. Arad
URL (if any):  http://gaia.ecs.csus.edu/~arad/csc142

Catalog Description

Design and performance issues of computers. Instruction set architecture, computer arithmetic, processor design, survey of contemporary architectures, interfacing I/O devices, hierarchical memory design and analysis, parallelism and multiprocessing, distributed systems, techniques for enhancing performance, and an introduction to EDA tools for design and verification of computers. Design and simulation of a microcomputer in an HDL. Cross-listed as CPE 142, and can be taken only once for credit. Prerequisite: CSc 137 OR CpE 166 and CpE 185.

Textbook


References


Course Goals

1. Provide students with a thorough understanding of design and performance issues of computers including arithmetic unit design tradeoffs, control unit design tradeoffs, CPU instruction set design issues, CPU datapath design issues, input/output interface design, memory hierarchy, and multiple processors.
2. Familiarize students with design and simulation of computer systems using a Hardware Description Language
3. Students will learn how to evaluate the performance of computers

Prerequisites by Topic

Thorough understanding of:
• Combinational circuit design
• Sequential circuit design
• Machine language programming
• Instruction execution cycle
• Memory internal organization

Basic Understanding of:
• CPU organization
• Control unit design
• Memory hierarchy
• Bus cycle
• I/O interface
• Direct memory access

Exposure to:
• Computer arithmetic
• Instruction pipelining
• Multiprocessor architecture
• A Hardware Description Language

Major Topics Covered in the Course

1. History and Overview (1 hour)
2. Review of Verilog HDL (4 hours)
3. Instruction Set Architecture (1 hour)
4. Computer Arithmetic (4 hours)
5. CPU architecture including datapath and control unit design (10 hours)
6. A survey of contemporary architectures including graphics and computing GPUs (2 hours)
7. Interfacing and communication (5 hours)
8. Memory system architecture including virtual memory and interleaved memory (3 hours)
9. Cache memory implementation and performance (6 hours)
10. Performance evaluation and enhancements (3 hours)
11. Parallelism and Instruction Level Parallelism (3 hours)
12. Introduction to distributed systems (3 hours)

Outcomes

Thorough understanding of:
• Instruction pipelining
• Processor design
• Memory hierarchy and optimization

Basic Understanding of:
• Instruction set architecture
• Integer and floating point arithmetic
• Branch prediction and speculative execution
• Super scalar and super pipelined instruction datapath
• Improving memory bandwidth (memory architecture)
• Improving data transfer rate (bus architecture)
• Performance evaluation

Exposure to:
• The role of compiler optimization in enhancing performance
• Data coherency in multiprocessor systems
• Introduction to parallel architectures
• Introduction to instruction-level parallelism
• Introduction to distributed systems
• EDA tools for design and simulation of computers

Laboratory projects

1. Introduction to Synopsys VCS Verilog Simulator (1 week)
2. Design and simulation of hardware components using Verilog HDL (3-4 weeks)
3. Students will design and simulate a microcomputer using Verilog HDL as part of the term project (5-6 weeks)

Estimated Curriculum Category Content (Semester hours)

<table>
<thead>
<tr>
<th>Area</th>
<th>Core</th>
<th>Advanced</th>
<th>Area</th>
<th>Core</th>
<th>Advanced</th>
</tr>
</thead>
<tbody>
<tr>
<td>Algorithms</td>
<td></td>
<td></td>
<td>Data Structures</td>
<td></td>
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<tr>
<td>Software Design</td>
<td></td>
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<td>Prog. Languages</td>
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<tr>
<td>Comp. Arch.</td>
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<td>3.0</td>
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Oral and Written Communications

Students in each team present their term project results in a grammatically correct technical report.

Social and Ethical Issues

No significant component

Theoretical Content

This is the undergraduate advanced computer architecture/organization elective course for the computer science degree. The course covers the theory of space vs. time optimization of arithmetic algorithm design, instruction pipelining, parallel vs. pipelining, cache memory coherency, and instruction level parallelism.

Problem Analysis
Alternative arithmetic algorithms and their implementation area vs. time trade offs are analyzed; various alternative CPU datapaths and their performance trade offs are analyzed; the pros and cons of CPU control design alternatives are analyzed; the effect of various memory system organizations on the average CPU memory access time is analyzed; impact of branch prediction and compiler optimization on CPI is analyzed.

Solution Design

Various arithmetic algorithms (adder, multiplier, etc.) design. Alternative control unit designs; Cache memory design, design using Verilog HDL, design of datapath (e.g., CPU, cache, etc.)

Assessment Plan

- Evaluation of selected exam questions.
- Evaluation of the Term Project

Relationship between the Course Outcomes and Program outcomes

<table>
<thead>
<tr>
<th>Program Outcomes</th>
<th>Mapping from Course Outcomes to Program Outcomes</th>
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</thead>
<tbody>
<tr>
<td>a</td>
<td>Students will design and analyze different components of a microcomputer</td>
</tr>
<tr>
<td>b</td>
<td>Students will learn how to evaluate the performance of a computer system</td>
</tr>
<tr>
<td>e</td>
<td>Students, in a team environment, will design and simulate a microcomputer based on a given instruction set in a Hardware Description Language and analyze its performance</td>
</tr>
<tr>
<td>g</td>
<td>Students in each team will present their term project results in a grammatically correct technical report</td>
</tr>
</tbody>
</table>

Revised by Behnam Arad, 10/18/2009
Prerequisite Revised 4/19/10
California State University, Sacramento  
COLLEGE OF ENGINEERING AND COMPUTER SCIENCE

COURSE APPROVAL CHECKLIST

Please answer all questions (enter NA if not applicable)

1. Course number and title: CPE 142, Advanced Computer Organization

2. Old course number and title: NA

3. Name of person in charge: Behnam S. Arad

4. Is the course X required ___ elective ___ service/GE (CPE 142 is required for CPE majors)

5. Check as appropriate: _____ new _____ change from 96/196/296

   X Change in description to reflect change in content
   X Change in prerequisite
   _____ Change in course format (e.g. lectures to lecture/lab)
   _____ Minor editing change in description
   _____ Change in number
   _____ Change in title

6. If offered as 96/196/296: ___NA___ number of times ___NA___ average enrollment

7. Does the proposed change or addition cause a significant increase in the use of College or University resources (lab room, computer facilities, faculty, etc.)? ___ No ___ If yes, attach description of resources needed, including lab room number if appropriate, and verify that these resources are available.

8. For all changes (except change in number, title, or minor editing change in description), attach and check off here:

   X detailed syllabus X justification X old description

9. If there are related course changes, state numbers here and submit as a package: _________ CSC 142

10. Date of department curriculum committee approval (if any): CPE 04/15/09 (desc change)

11. Date of department faculty approval (if any): __________________________

FOR NEW COURSES (Including changes from 96/196/296):

Is the course related to or similar to any existing course? _____ If so, include explanation with justification.

Describe the target group of students: ____________________________________________

NOTE:

1. Syllabus should include title, author and date of text, name of instructor, main topics, amount or percentage of time devoted to each, description of special features such as term projects, and ABET or CAC content category.

2. For required courses the justification must indicate how the new course fits into the overall curriculum and why changes are being made or the new course is being added.