- Package Options Include Plastic and Ceramic DIPs and Ceramic Flat Packages
- Dependable Texas Instruments Quality and Reliability

### description

The '76 contains two independent J-K flip-flops with individual J-K, clock, preset, and clear inputs. The '76 is a positive-edge-triggered flipflop. J-K input is loaded into the master while the clock is high and transferred to the slave on the high-to-low transition. For these devices the J and K inputs must be stable while the clock is high.

The 'LS76A contain two independent negativeedge-triggered flip-flops. The J and K inputs must be stable one setup time prior to the highto-low clock transition for predicatble operation. The preset and clear are asynchronous active low inputs. When low they override the clock and data inputs forcing the outputs to the steady state levels as shown in the function table.

The SN5476 and the SN54LS76A are characterized for operation over the full military temperature range of -55 °C to 125 °C. The SN7476 and the SN74LS76A are characterized for operation from 0 °C to 70 °C.

SN5476, SN54LS76A . . . J PACKAGE SN7476 . . . N PACKAGE SN74LS76A . . . D OR N PACKAGE (TOP VIEW)

1 CLK 1 16 1K   1 PRE 2 15 10   1 CLR 3 14 10   1 J 4 13 GND   VCC 5 12 2K   2CLK 6 11 20   2 PRE 7 10 20   2 CLR 8 9 2J		•••••	,	
	1 PRE 1 CLR 1 J VCC 2 CLK 2 PRE	- 3 4 5	15 14 13	] 10 ] 10 ] GND ] 2K ] 20 ] 20
	2 0 1 1 1	<u> </u>		1

'76 FUNCTION TABLE										
	IN	OUT	UTS							
PRE	CLR	CLK	J	к	Q	ā				
L	н	×	х	х	н	L				
н	L	×	х	х	L L	н				
L	L	х	х	х	нt	HT				
н	н	л	L	L	0 <sub>0</sub>	ā <sub>0</sub>				
н	н	л	н	Ł	н	L				
н	н	л	L	н	L	н				
н	н	л	н	н	TOG	GLE				

LS76A

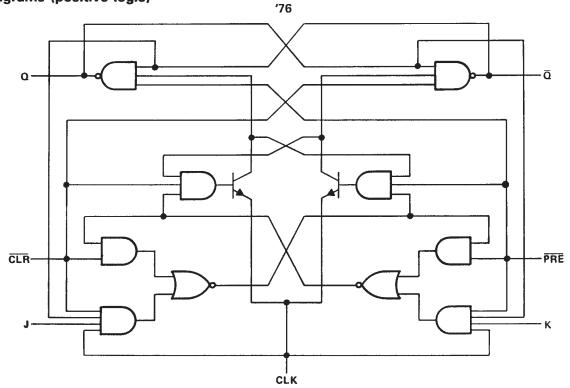
		FUNCT		ADLE		
	IN	OUTPUTS				
PRE	CLR	CLK	J	к	Q	ā
L	н	х	х	Х	н	L
н	L	х	х	х	L	н
L	L	×	х	х	н†	нţ
н	н	÷.	L	L	Q0	$\overline{\alpha}_0$
н	н	ţ	н	L	н	Ļ
н	н	Ļ	L	н	L	н
н	н	Ļ	н	н	TOG	GLE
н	н	н	х	х	0 <sub>0</sub>	$\overline{\Omega}_0$

<sup>†</sup> This configuration is nonstable; that is, it will not persist when either preset or clear returns to its inactive (high) level.

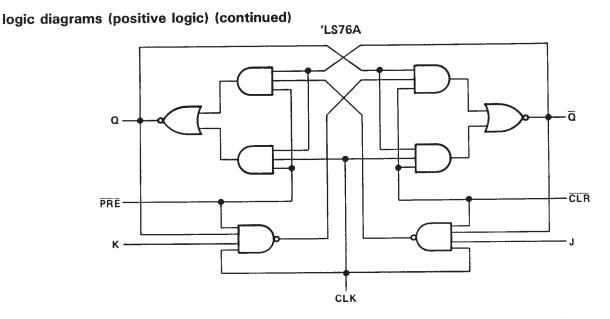


# SN5476, SN54LS76A SN7476, SN74LS76A DUAL J-K FLIP-FLOPS WITH PRESET AND CLEAR SDLS121 – DECEMBER 1983 – REVISED MARCH 1988

# logic diagrams (positive logic)





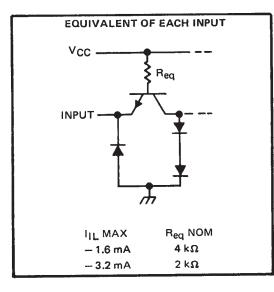


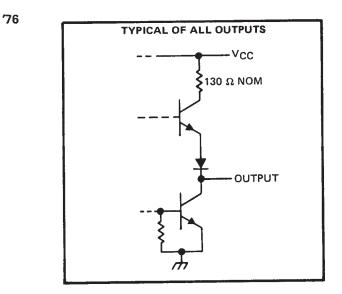
# logic symbols<sup>†</sup>



<sup>†</sup>These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

### schematics of inputs and outputs

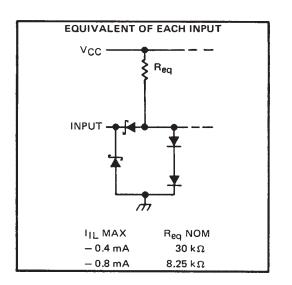


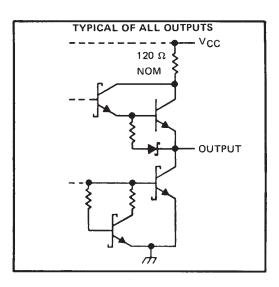




# SN5476, SN54LS76A SN7476, SN74LS76A DUAL J-K FLIP-FLOPS WITH PRESET AND CLEAR SDLS121 – DECEMBER 1983 – REVISED MARCH 1988

# schematics of inputs and outputs (continued)





### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

'LS76A

Supply voltage, V <sub>CC</sub> (see Note 1)	7 V
Input voltage: '76	
'LS76A	7 V
Operating free-air temperature range: SN54' 55 °C to 12	5°C
SN74' 0°C to 7	0°C
Storage temperature range	0°C

NOTE 1: Voltage values are with respect to network ground terminal.



### recommended operating conditions

			SN5476			SN7476	6		
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
VIH	High-level input voltage	2			2			V	
VIL	Low-level input voltage			0.8			0.8	V	
ЮН	High-level output current			0.4			- 0.4	mA	
IOL	Low-level output current				16			16	mA
		CLK high	20		-	20			Ţ
tw	Pulse duration	CLK low	47			47			ns
		PRE or CLR low	25			25			
t <sub>su</sub>	Input setup time before CLK †		0			0			ns
th	Input hold time-data after CLK ↓		0			0			ns
TA	Operating free-air temperature		- 55		125	0		70	°C

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

				evet		SN5476			SN7476		UNIT	
PAR	AMETER		TEST CONDITIO	ONS	MIN	TYP‡	MAX	MIN	TYP‡	MAX	0	
VIK		V <sub>CC</sub> = MIN,	lj = − 12 mA				- 1.5			- 1.5	V	
Vон		V <sub>CC</sub> = MIN, I <sub>OH</sub> = - 0.4 mA	V <sub>IH</sub> = 2 V,	V <sub>1L</sub> = 0.8 V,	2.4	3.4		2.4	3.4		v	
VOL		V <sub>CC</sub> = MIN, I <sub>OL</sub> = 16 mA	V <sub>IH</sub> = 2 V,	V <sub>IL</sub> = 0.8 V,		0.2	0.4		0.2	0.4	v	
ξį.		V <sub>CC</sub> = MAX,	V <sub>I</sub> = 5.5 V				1			1	mA	
	J or K		N - 0 4 M				40			40	μA	
ЧН	All other	V <sub>CC</sub> = MAX,	V <sub>I</sub> = 2.4 V				80			80	<u><u></u></u>	
	J or K						- 1.6			- 1.6	mA	
ηr	All other	V <sub>CC</sub> = MAX,	V <sub>I</sub> = 0.4 V				- 3.2			- 3.2	- IIIA	
los§		V <sub>CC</sub> = MAX			- 20		- 57	- 18		- 57	mA	
ICC#	THE PARTY OF THE P	V <sub>CC</sub> = MAX,	See Note 2			10	20		10	20	mA	

<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

<sup>‡</sup>All typical values are at  $V_{CC} = 5 V$ ,  $T_A = 25 °C$ .

§ Not more than one output should be shorted at a time.

¶Clear is tested with preset high and preset is tested with clear high.

#Average per flip-flop.

NOTE 2: With all outputs open, I<sub>CC</sub> is measured with the Q and Q outputs high in turn. At the time of measurement, the clock input is grounded.

switching characteristics,	, VCC = 5 \	$V, T_A = 25^{\circ}C$	(see note 3)
----------------------------	-------------	------------------------	--------------

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	түр	MAX	UNIT	
fmax				15	20		MHz	
tPLH		PRE or CLR	$Q$ or $\overline{Q}$			16	25	ns
<sup>t</sup> PHL	FRE OF CER		$R_{L} = 400 \Omega$ , $C_{L} = 15 pF$		25	40	ns	
<sup>t</sup> PLH	CLK	$Q$ or $\overline{Q}$	]		16	25	ns	
<sup>t</sup> PHL	ULK				25	40	ns	

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



### SN5476, SN54LS76A SN7476, SN74LS76A DUAL J-K FLIP-FLOPS WITH PRESET AND CLEAR SDLS121 – DECEMBER 1983 – REVISED MARCH 1988

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#### recommended operating conditions

			S	N54LS7	6A	SN74LS76A			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Vcc	Supply voltage		4.5	5	5.5	4.75	5	5.75	V
VIH	High-level input voltage					2			V
VIL	Low-level input voltage				0.7			0.8	V
ЮН	High-level output current			- 0.4			- 0.4	mA	
IOL	Low-level output current	Î		4			8	mA	
fclock	Clock frequency		0		30	0		30	MHz
		CLK high	20			20			ns
tw	Pulse duration	PRE or CLR low	25	·		25			115
		data high or low	20			20			
t <sub>su</sub>	Setup time before CLK↓	CLR inactive	20			20			ns
	PRE inactive		25			25			
t <sub>h</sub>	Hold time-data after CLK		0		-	0			ns
TA	Operating free-air temperature		- 55		125	0		70	°C

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

					S	N54LS7	6A	S	N74LS7	6A	UNIT
	PARAMETER		TEST CONDITIO	DNS	MIN	түр‡	MAX	MIN	түр‡	MAX	UNIT
VIK		V <sub>CC</sub> = MIN,	lı = — 18 mA				- 1.5	<u> </u>		- 1.5	V
vон		V <sub>CC</sub> = MIN, I <sub>OH</sub> = − 0.4 mA	V <sub>IH</sub> = 2 V,	VIL = MAX,	2.5	3.4		2.7	3.4		v
		V <sub>CC</sub> = MIN, I <sub>OL</sub> = 4 mA	VIL = MAX,	V <sub>IH</sub> = 2 V,		0.25	0.4		0.25	0.4	v
VOL		V <sub>CC</sub> = MIN, i <sub>OL</sub> = 8 mA	V <sub>IL</sub> = MAX,	V <sub>IH</sub> = 2 V,					0.35	0.5	
	J or K						0.1			0.1	<u> </u>
I <sub>E</sub>	CLR or PRE	V <sub>CC</sub> = MAX,	V <sub>1</sub> = 7 V				0.3			0.3	mA
	CLK				0.4					0.4	
	J or K						20			20	
ЧΗ	CLR or PRE	V <sub>CC</sub> = MAX,	V <sub>1</sub> = 2.7 V				60			60	μA
••••	CLK						80			80	
	J or K				- 0.		- 0.4			- 0.4	mA
μL	All other	$-V_{CC} = MAX,$	∨ <sub>1</sub> = 0.4 ∨				- 0.8			- 0.8	A
los§	<u> </u>	V <sub>CC</sub> = MAX,	See Note 4		- 20		- 100	- 20		- 100	mA
	Total)	V <sub>CC</sub> = MAX,	See Note 2			4	6		4	6	mA

<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at  $V_{CC} = 5 V$ ,  $T_A = 25^{\circ}C$ .

§Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

NOTE 2: With all outputs open, I<sub>CC</sub> is measured with the Q and Q outputs high in turn. At the time of measurement, the clock input is grounded.

NOTE 4: For certain devices where state commutation can be caused by shorting an output to ground, an equivalent test may be performed with V<sub>O</sub> = 2.25 V and 2.125 V for the 54 family and the 74 family, respectively, with the minimum and maximum limits reduced to one half of their stated values.

# switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	түр	МАХ	UNIT
fmax				30	45		MHz
tPLH			$R_L = 2 k\Omega$ , $C_L = 15 pF$		15	20	ns
<sup>t</sup> PHL	PRE, CLR or CLK	Q or Q	-		15	20	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



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5962-9557501QFA   ACTIVE   CDIP   J   16   1   TBD   A42 SNPB   N / A for Pkg Type     5962-9557501QFA   ACTIVE   CFP   W   16   1   TBD   A42   N / A for Pkg Type     5962-9557501QFA   ACTIVE   CDIP   J   16   1   TBD   A42   N / A for Pkg Type     7601301EA   ACTIVE   CDIP   J   16   1   TBD   A42 SNPB   N / A for Pkg Type     JM38510/00204BEA   ACTIVE   CDIP   J   16   1   TBD   A42 SNPB   N / A for Pkg Type     SN5476J   ACTIVE   CDIP   J   16   1   TBD   A42 SNPB   N / A for Pkg Type     SN5476J   ACTIVE   CDIP   J   16   1   TBD   A42 SNPB   N / A for Pkg Type     SN541S76AJ   ACTIVE   CDIP   J   16   1   TBD   A42 SNPB   N / A for Pkg Type     SN541S76AJ   ACTIVE   CDIP   J   16   1   TBD	Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finis	h MSL Peak Temp <sup>(3)</sup>
5962-9557501QFA   ACTIVE   CFP   W   16   1   TBD   A42   N / A for Pkg Type     7601301EA   ACTIVE   CDIP   J   16   1   TBD   A42 SNPB   N / A for Pkg Type     7601301EA   ACTIVE   CDIP   J   16   1   TBD   A42 SNPB   N / A for Pkg Type     JM38510/00204BEA   ACTIVE   CDIP   J   16   1   TBD   A42 SNPB   N / A for Pkg Type     JM38510/00204BEA   ACTIVE   CDIP   J   16   1   TBD   A42 SNPB   N / A for Pkg Type     SN5476J   ACTIVE   CDIP   J   16   1   TBD   A42 SNPB   N / A for Pkg Type     SN5476J   ACTIVE   CDIP   J   16   1   TBD   A42 SNPB   N / A for Pkg Type     SN541S76AJ   ACTIVE   CDIP   J   16   1   TBD   A42 SNPB   N / A for Pkg Type     SN541S76AJ   ACTIVE   CDIP   J   16   1   TBD	5962-9557501QEA	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
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	SNJ54LS76AW	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type

 $^{(1)}$  The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details. TBD: The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

# PACKAGE OPTION ADDENDUM



**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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J (R-GDIP-T\*\*) 14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within MIL STD 1835 GDFP1-F16 and JEDEC MO-092AC



# N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- $\triangle$  The 20 pin end lead shoulder width is a vendor option, either half or full width.



D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.

Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.

E. Reference JEDEC MS-012 variation AC.



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