Monolithic N-Channel JFET Dual

PRODUCT SUMMARY

| $V_{GS(\text{off})}$ (V) | $V_{BR\text{GSS}}$ Min (V) | $g_{fs}$ Min (mS) | $I_G$ Max (pA) | $|V_{G1} - V_{G2}|$ Max (mV) |
|------------------------|-------------------------|-----------------|----------------|-------------------------------|
| $-1.0$ to $-4.5$       | $-50$                   | $1$             | $-50$          | $25$                          |

FEATURES

- Monolithic Design
- High Slew Rate
- Low Offset/Drift Voltage
- Low Gate Leakage: 5 pA
- Low Noise: 9 nV/√Hz
- High CMRR: 100 dB

BENEFITS

- Tight Differential Match vs. Current
- Improved Op Amp Speed, Settling Time Accuracy
- Minimum Input Error/Trimming Requirement
- Insignificant Signal Loss/Error Voltage
- High System Sensitivity
- Minimum Error with Large Input Signal

APPLICATIONS

- Wideband Differential Amps
- High-Speed, Temp-Compensated, Single-Ended Input Amps
- High Speed Comparators
- Impedance Converters

DESCRIPTION

The low cost 2N3958 JFET dual is designed for high-performance differential amplification for a wide range of precision test instrumentation applications. This series features tightly matched specs, low gate leakage for accuracy, and wide dynamic range with $I_G$ guaranteed at $V_{DG} = 20$ V.

The hermetically-sealed TO-71 package is available with full military processing (see Military Information and the 2N5545/5546/5547JANTX/JANTXV data sheet).

For similar products see 2N5196/5197/5198/5199, the low-noise U/SST401 series, the high-gain 2N5911/5912, and the low-leakage U421/423 data sheets.

ABSOLUTE MAXIMUM RATINGS

- Gate-Drain, Gate-Source Voltage: $-50$ V
- Gate Current: $50$ mA
- Lead Temperature ($1/16$" from case for 10 sec.): $300$ °C
- Storage Temperature: $-65$ to $200$ °C
- Operating Junction Temperature: $-55$ to $150$ °C

Power Dissipation:
- Per Side: $250$ mW
- Total: $500$ mW

Notes:
- a. Derate $2$ mW/°C above $85$ °C
- b. Derate $4$ mW/°C above $85$ °C
### SPECIFICATIONS (TA = 25°C UNLESS OTHERWISE NOTED)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Conditions</th>
<th>Limits</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Static</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Gate-Source Breakdown Voltage</td>
<td>V(BR)GSS</td>
<td>IG = -1 μA, VDS = 0 V</td>
<td>-50</td>
<td>V</td>
</tr>
<tr>
<td>Gate-Source Cutoff Voltage</td>
<td>VGs(Off)</td>
<td>VDS = 20 V, ID = 1 nA</td>
<td>-1.0</td>
<td>V</td>
</tr>
<tr>
<td>Saturation Drain Current</td>
<td>IDSS</td>
<td>VGS = -30 V, VDS = 0 V</td>
<td>0.5</td>
<td>mA</td>
</tr>
<tr>
<td>Gate Reverse Current</td>
<td>IGSS</td>
<td>TA = 150°C</td>
<td>-10</td>
<td>pA</td>
</tr>
<tr>
<td>Gate Operating Current</td>
<td>IG</td>
<td>VDG = 20 V, ID = 200 μA</td>
<td>-0.5</td>
<td>mA</td>
</tr>
<tr>
<td>Gate-Source Voltage</td>
<td>VG</td>
<td>VDG = 20 V, ID = 200 μA</td>
<td>-0.5</td>
<td>V</td>
</tr>
<tr>
<td><strong>Dynamic</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Common-Source Forward Transconductance</td>
<td>gfs</td>
<td>VDS = 20 V, VGS = 0 V f = 1 kHz</td>
<td>1</td>
<td>mS</td>
</tr>
<tr>
<td>Common-Source Output Conductance</td>
<td>gos</td>
<td>VDS = 20 V, VGS = 0 V f = 1 kHz</td>
<td>2</td>
<td>μS</td>
</tr>
<tr>
<td>Common-Source Input Capacitance</td>
<td>CGS</td>
<td>VDS = 20 V, VGS = 0 V f = 1 MHz</td>
<td>3</td>
<td>pF</td>
</tr>
<tr>
<td>Common-Source Reverse Transfer Capacitance</td>
<td>CRSS</td>
<td>VDS = 20 V, VGS = 0 V f = 1 MHz</td>
<td>1</td>
<td>pF</td>
</tr>
<tr>
<td>Drain-Gate Capacitance</td>
<td>CGD</td>
<td>VDG = 10 V, IS = 0 , f = 1 MHz</td>
<td>1.5</td>
<td></td>
</tr>
<tr>
<td>Equivalent Input Noise Voltage</td>
<td>en</td>
<td>VDS = 20 V, VGS = 0 V f = 1 kHz</td>
<td>9</td>
<td>nV/√Hz</td>
</tr>
<tr>
<td>Noise Figure</td>
<td>NF</td>
<td>VDS = 20 V, VGS = 0 V f = 100 Hz, RG = 10 MΩ</td>
<td>0.5</td>
<td>dB</td>
</tr>
<tr>
<td><strong>Matching</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Differential Gate-Source Voltage</td>
<td></td>
<td>VDG = 20 V, ID = 200 μA</td>
<td>15</td>
<td>mV</td>
</tr>
<tr>
<td>Gate-Source Voltage Differential Change with Temperature</td>
<td>Δ(VGS1-VGS2)/ΔT</td>
<td>VDG = 20 V, ID = 200 μA TA = -55 to 125°C</td>
<td>20</td>
<td>μV/°C</td>
</tr>
<tr>
<td>Saturation Drain Current Ratio</td>
<td>IDSS1/IDSS2</td>
<td>VDS = 20 V, VGS = 0 V</td>
<td>0.85</td>
<td></td>
</tr>
<tr>
<td>Transconductance Ratio</td>
<td>gfs1/gfs2</td>
<td>VDS = 20 V, VGS = 0 V f = 1 kHz</td>
<td>0.85</td>
<td></td>
</tr>
<tr>
<td>Differential Output Conductance</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Differential Gate Current</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Common Mode Rejection Ratio</td>
<td>CMRR</td>
<td>VDG = 20 V, ID = 200 μA TA = -55 to 125°C</td>
<td>100</td>
<td>dB</td>
</tr>
</tbody>
</table>

**Notes**
- a. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- b. Pulse test: PW ≤ 300 μs duty cycle ≤ 3%.
- c. This parameter not registered with JEDEC.

---

www.vishay.com

www.vishay.com Document Number: 70256

S-04031—Rev. B, 04-Jun-01

8-2
TYPICAL CHARACTERISTICS \( (T_A = 25^\circ C \text{ UNLESS OTHERWISE NOTED}) \)

Drain Current and Transconductance vs. Gate-Source Cutoff Voltage

Gate Leakage Current

Output Characteristics

Output Characteristics
TYPICAL CHARACTERISTICS (T_A = 25°C UNLESS OTHERWISE NOTED)

- **Transfer Characteristics**
  - V_GS(off) = –2 V
  - V_D = 20 V

- **Gate-Source Differential Voltage vs. Drain Current**
  - V_D = 20 V
  - V_A = 25°C

- **Voltage Differential with Temperature vs. Drain Current**
  - V_D = 20 V
  - ΔT_A = 25 to 125°C
  - ΔT_A = –55 to 25°C

- **Common Mode Rejection Ratio vs. Drain Current**
  - CMRR = 20 log (ΔV_D = 10 – 20 V)
  - ΔV_D = 5 – 10 V

- **Circuit Voltage Gain vs. Drain Current**
  - V_D = 20 V
  - V_GS(off) = –3 V

- **On-Resistance vs. Drain Current**
  - V_D = 20 V
  - V_GS(off) = –2 V

- **2N3958**
  - Vishay Siliconix
  - www.vishay.com
  - Document Number: 70256
  - S-04031 — Rev. B, 04-Jun-01
TYPICAL CHARACTERISTICS (TA = 25°C UNLESS OTHERWISE NOTED)

Common-Source Input Capacitance vs. Gate-Source Voltage

Common-Source Reverse Feedback Capacitance vs. Gate-Source Voltage

Equivalent Input Noise Voltage vs. Frequency

Output Conductance vs. Drain Current

Common-Source Forward Transconductance vs. Drain Current

On-Resistance and Output Conductance vs. Gate-Source Cutoff Voltage
Notice

Specifications of the products displayed herein are subject to change without notice. Vishay Intertechnology, Inc., or anyone on its behalf, assumes no responsibility or liability for any errors or inaccuracies.

Information contained herein is intended to provide a product description only. No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document. Except as provided in Vishay’s terms and conditions of sale for such products, Vishay assumes no liability whatsoever, and disclaims any express or implied warranty, relating to sale and/or use of Vishay products including liability or warranties relating to fitness for a particular purpose, merchantability, or infringement of any patent, copyright, or other intellectual property right.

The products shown herein are not designed for use in medical, life-saving, or life-sustaining applications. Customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Vishay for any damages resulting from such improper use or sale.