CPE 151: CMOS AND DIGITAL VLSI DESIGN

In Workflow

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10. Registrar's Office (wlindsey@csus.edu)
11. PeopleSoft (PeopleSoft@csus.edu)

Approval Path

1. Fri, 24 Apr 2020 21:08:22 GMT
   Mahyar Zarghami (mahyar.zarghami): Approved for EEE Committee Chair
2. Thu, 28 May 2020 21:08:11 GMT
   Fethi Belkhouche (fbelkhou): Approved for EEE Chair
3. Fri, 18 Sep 2020 03:30:17 GMT
   Gareth Figgess (figgess): Approved for ECS College Committee Chair
4. Fri, 18 Sep 2020 17:46:49 GMT
   Kevan Shafizadeh (kevan): Approved for ECS Dean

Date Submitted: Wed, 22 Apr 2020 19:41:20 GMT

Viewing: CPE 151 : CMOS and Digital VLSI Design

Last edit: Fri, 11 Sep 2020 17:11:30 GMT

Changes proposed by: Praveen Meduri (219708594)

Contact(s):

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Catalog Title:
CMOS and Digital VLSI Design

Class Schedule Title:
CMOS and Digital VLSI Design

Academic Group: (College)
ECS - Engineering & Computer Science

Academic Organization: (Department)
Electrical and Electronic Engineering

Will this course be offered through the College of Continuing Education (CCE)?
No

Catalog Year Effective:
Spring 2021 (2021/2022 Catalog)

Subject Area: (prefix)
CPE - Computer Engineering

Catalog Number: (course number)
151

Course ID: (For administrative use only.)
110601

Units:
3

In what term(s) will this course typically be offered?
Fall, Spring

Does this course require a room for its final exam?
Yes, final exam requires a room

Does this course replace an existing experimental course?
No

This course complies with the credit hour policy:
Yes

Justification for course proposal:
Minor modifications to an existing course. Specifically, only the catalog description is being modified.

While the course is being currently taught using upto date industry standard software, the existing catalog description refers to older tools that are not currently in use for this course. This modification is to enhance the currency of the catalog description.

Course Description: (Not to exceed 80 words and language should conform to catalog copy.)
Introduction to CMOS logic gates and the design of CMOS combinational and sequential functions at the gate level, including CMOS memory. CMOS transistor theory is covered including: DC equations, threshold voltage, body effect, subthreshold region, channel length modulation, tunneling, and punch through. A basic exposure to VLSI includes: CMOS processing technology, layout, and CMOS logic design including power, delay and timing considerations. Students will use industry standard Computer Aided Design tools to verify designs and layouts.

Are one or more field trips required with this course?
No

Fee Course?
No

Is this course designated as Service Learning?
No

Does this course require safety training?
No

Does this course require personal protective equipment (PPE)?
No

Does this course have prerequisites?
Yes

Prerequisite:
CPE 64 and EEE 108.

Prerequisites Enforced at Registration?
Yes

Does this course have corequisites?
No

Graded:
Letter

Approval required for enrollment?
No Approval Required

Course Component(s) and Classification(s):
Lecture

Lecture Classification

CS#02 - Lecture/Discussion (K-factor=1WTU per unit)

Lecture Units

3

Is this a paired course?

No

Is this course crosslisted?

No

Can this course be repeated for credit?

No

Can the course be taken for credit more than once during the same term?

No

Description of the Expected Learning Outcomes: Describe outcomes using the following format: 'Students will be able to: 1), 2), etc.'

After taking this course, students will be able to:

1) Apply basic device physics that dictate the functionality of CMOS circuits

2) Analyze and design CMOS logic gates at the transistor level, including memory

3) Explore tradeoffs between performance, power, and area for CMOS digital circuits

4) Use industry standard physical design tool to layout CMOS logic circuits

5) Describe issues and make tradeoffs for large "system on a chip" designs

Assessment Strategies: A description of the assessment strategies (e.g., portfolios, examinations, performances, pre-and post-tests, conferences with students, student papers) which will be used by the instructor to determine the extent to which students have achieved the learning outcomes noted above.

Tentative assessment components:

1. In-class and/or online quizzes (Used to Assess Learning Outcome #s 1 and 2)
2. Software projects (Used to assess Learning Outcome #s 2, 3 and 4)
3. Midterm, Final Exams (Used to Assess Learning Outcome #s 1, 2, 3 and 5)
4. Graded/ungraded Homeworks (Used to Assess Learning Outcome #s 1, 2, 3)

Is this course required in a degree program (major, minor, graduate degree, certificate?)

Yes

Has a corresponding Program Change been submitted to Workflow?

No

Identify the program(s) in which this course is required:

Programs:
BS in Computer Engineering

Does the proposed change or addition cause a significant increase in the use of College or University resources (lab room, computer)?

No

Will there be any departments affected by this proposed course?

No

I/we as the author(s) of this course proposal agree to provide a new or updated accessibility checklist to the Dean's office prior to the semester when this course is taught utilizing the changes proposed here.

I/we agree

University Learning Goals

Undergraduate Learning Goals:

Competence in the disciplines

Is this course required as part of a teaching credential program, a single subject, or multiple subject waiver program (e.g., Liberal Studies, Biology) or other school personnel preparation program (e.g., School of Nursing)?

No

GE Course and GE Goal(s)

Is this a General Education (GE) course or is it being considered for GE?

No

Please attach any additional files not requested above:

0_CpE_151_Syllabus_S20.pdf

Key: 860