CPE/EEE 64 PAL Worksheet #10

VERILOG WORKSHEET -1

1) Verilog HDL is case-sensitive? True or False
2) Which keyword signifies the end of a module definition?
3) Which Keyword signifies the beginning of a block of statements?
4) Which of the following are legal Verilog identifiers? 632h,_6hft, A123,or

One can concatenate vectors, scalars, and part vectors to form other vectors. The concatenated vector is enclosed within braces. Commas separate the components –scalars, vectors, and part vectors. If a and b are 8- and 4-bit wide vectors, respectively and c is a scalar {a, b, c} stands for a concatenated vector of 13 bits width. The vector components are formed in the order shown – c is the least significant bit and a[7] the most significant bit and the other bits are in between in the order specified.

Example 1) For the snippet of code given below evaluate {b,c}

wire a = 1'b1;

wire b = 2'b10;

wire c = 3'b101;

{b,c} = 5'b10101;

5) For the snippet of code given below evaluate {b,a,2'b11}

wire a = 3'b101;

wire b = 2'b11;

wire c = 3'b011;

6) For the snippet of code given below evaluate {c,a,b,5'b10110}

wire a = 2'b11;

wire b = 5'b11100;

wire c = 3'b100;

When it is necessary to replicate vectors, scalars, etc., to form other vectors, the same can be arrived at in a compact manner using the repetition multiplier again through concatenation.

Example 2) If wire a=2'b10 then {3{a}} = 6'b101010.

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7) Evaluate {2{a},5{b}} if wire a = 3'b101; wire b = 2'b10;

A >> b The set of bits representing A are shifted right repeatedly b times.
A << b The set of bits representing A are shifted left repeatedly b times.

8) If A = 8'hD5 evaluate A >> 4 and A << 4.

Operator Type	Symbol
Logical negation	!
Bit wise negative	~
Reduction AND	&
Reduction NAND	~&
Reduction OR	|
Reduction NOR	~|
Reduction XOR	^
Reduction XNOR	~^

9) If A = 101, B = 011, and C = 010, what is the value of {A,B} | {B,C}.
10) If A = 1110, and B = 1011, what is the value of {A,(~B)}.