ASM Charts

An algorithmic state machine (ASM) diagram offers several advantages over state diagrams:

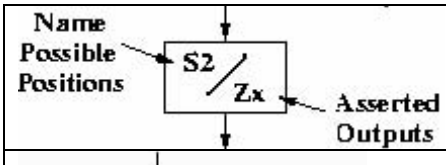
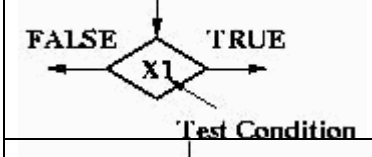
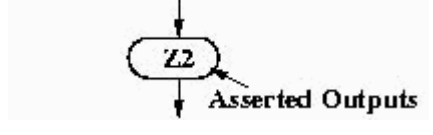
- For larger state diagrams, often are easier to interpret
- conditions for a *proper* state diagram are automatically satisfied
- may be easily converted to other forms

A key point to remember about ASM charts is that given a state, they do not enumerate all the possible inputs and outputs. Only the inputs that matter and the outputs that are *asserted* are indicated. It must be known whether a signal is *positive* or *negative* logic:

- Positive logic signals that are *high* are said to be *asserted*
- Negative logic signals that are *low* are said to be de*asserted*

The ASM Diagram Block

An ASM chart has an entry point and is constructed with blocks. A block is constructed with the following type of symbols.

	One state box. The state box has a name and lists outputs that are asserted when the system is in that state. These outputs are called synchronous or *Moore* type outputs.
	Optional decision box (es). A decision box may be conditioned on a signal or a test of some kind.
	Optional conditional output box (es). Such an output box indicates outputs that are conditionally asserted. These outputs are called asynchronous or *Mealy* outputs.

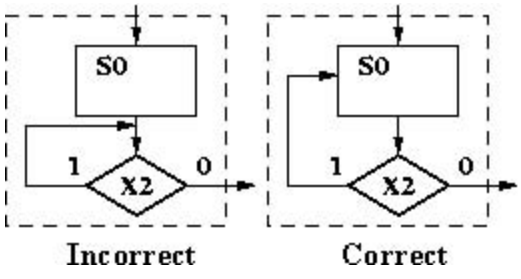
There is no rule saying that outputs are exclusively inside an a conditional output box or in a state box. An output written inside a state box is simply independent of the input, while in that state.

Certain Rules

The drawing of ASM charts must follow certain necessary rules:

- The entrance paths to an ASM block lead to only one state box
- Of 'N' possible exit paths, for each possible valid input combination, only one exit path can be followed, that is there is only one valid next state.

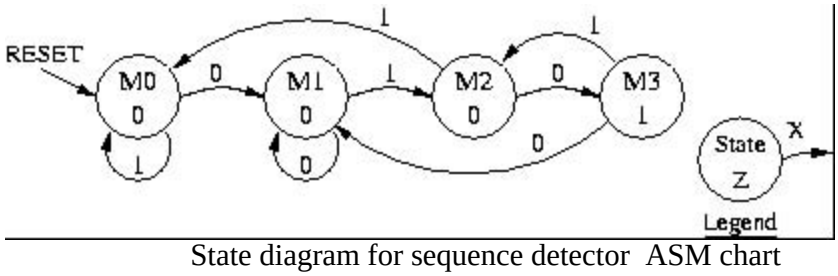
- No feedback internal to a state box is allowed. The following diagram indicates valid and invalid cases.



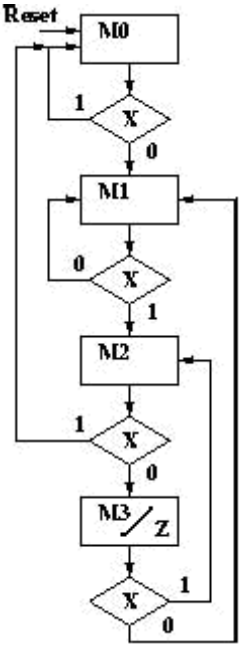
Sequence Detector Example

The use of ASM charts is a trade-off. While the mechanics of ASM charts do reduce clutter in significant designs, its better to use an ordinary state diagrams for simple state machines. Here is an example Moore type state machine with input X and output Z. Once the flag sequence is received, the output is asserted for one clock cycle.

The corresponding ASM chart is to the right. Note that unlike the state diagram which illustrates the output value for each arc, the ASM chart indicates when the output Z only when it is asserted.

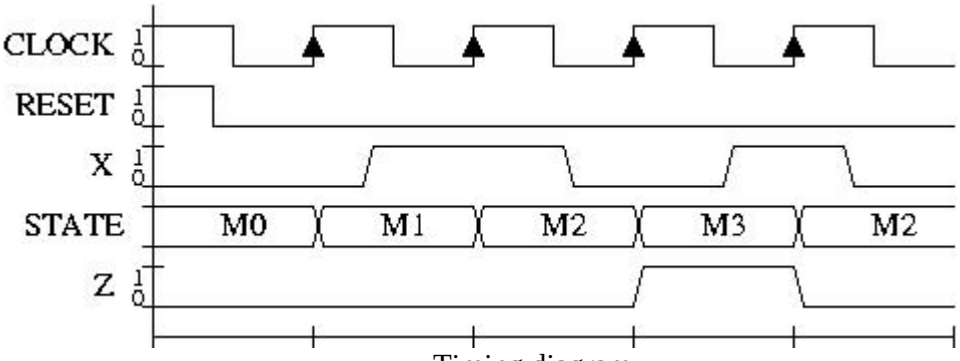


State diagram for sequence detector



ASM chart

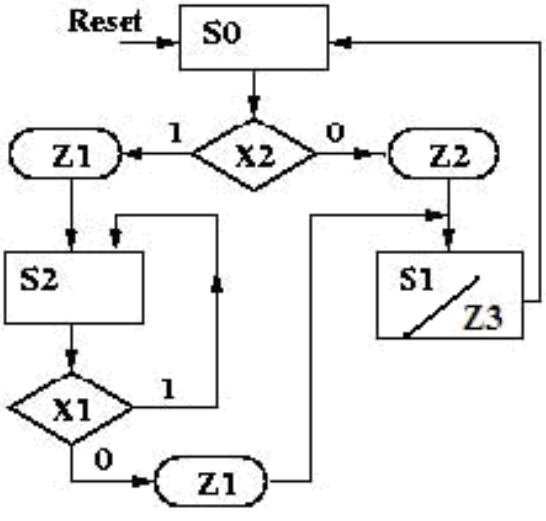
The following timing diagram illustrates the detection of the desired sequence. Here it is assumed that the state is updated with a *rising clock edge*. The key concept to observe is that regardless of the input, the output can only be asserted for one entire clock cycle.



Timing diagram

Asynchronous and Synchronous Output Example

The following is an example of an ASM chart with inputs X1 and X2, and outputs Z1, Z2 and Z3. In state S0 the outputs are immediately dependent on the input. In state S1, output Z3 is always asserted. In state S2, output Z1 is dependent on input X1 but Z2 is not asserted.



Example ASM chart