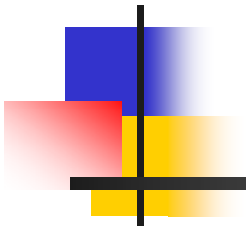
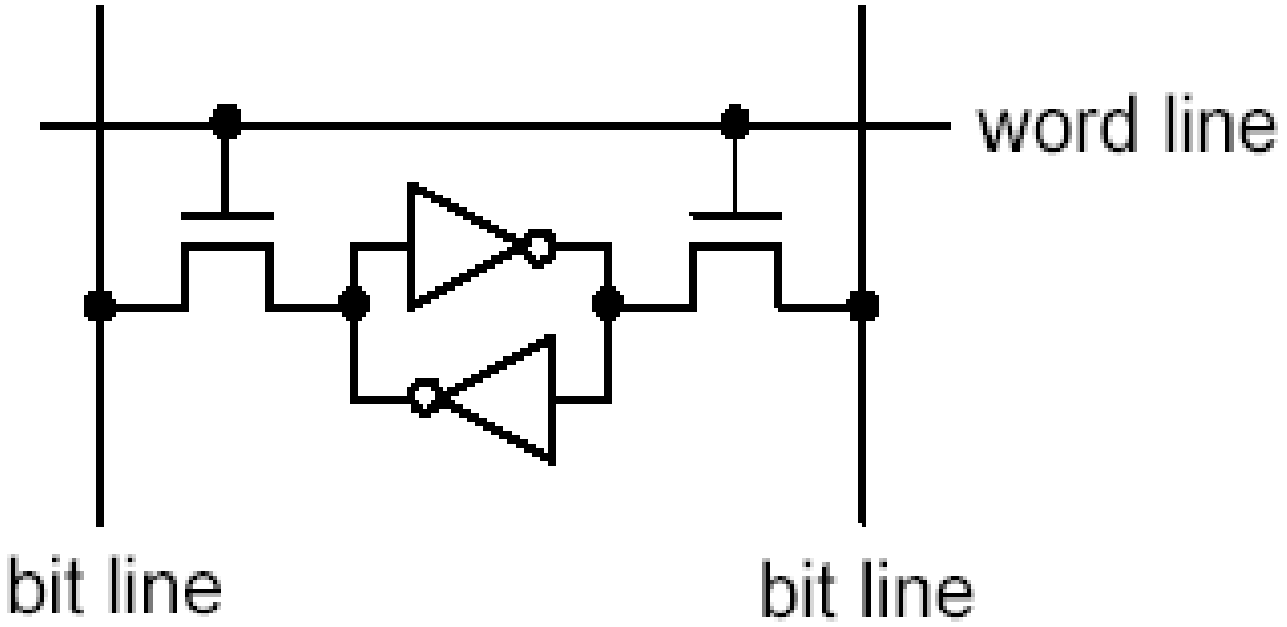


SRAM

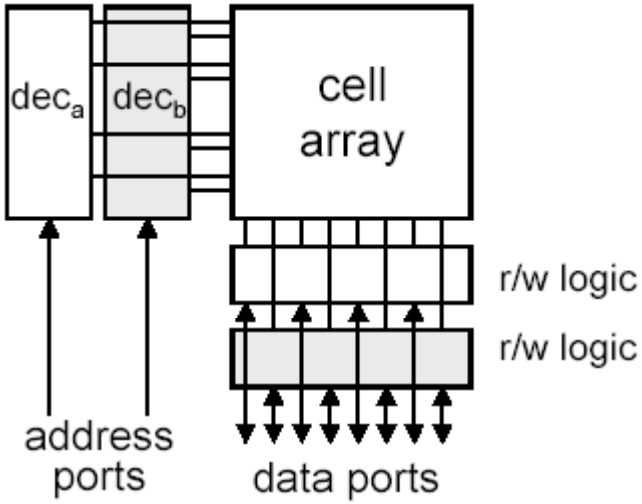
Dr. Jing Pang

SRAM Cell

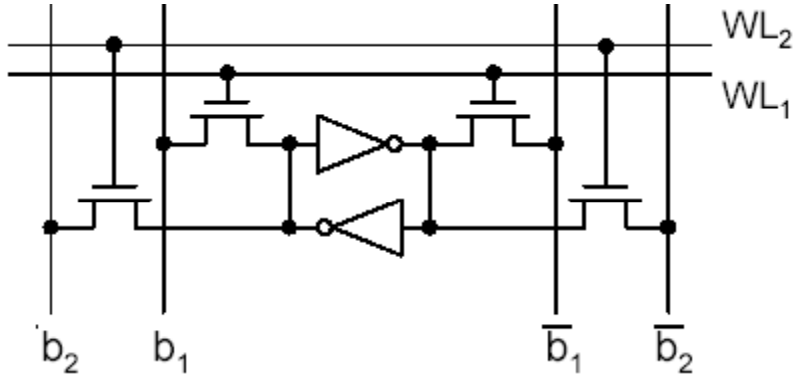


Dual-Port Memory

Add decoder, another set of read/write logic, bits lines, word lines:



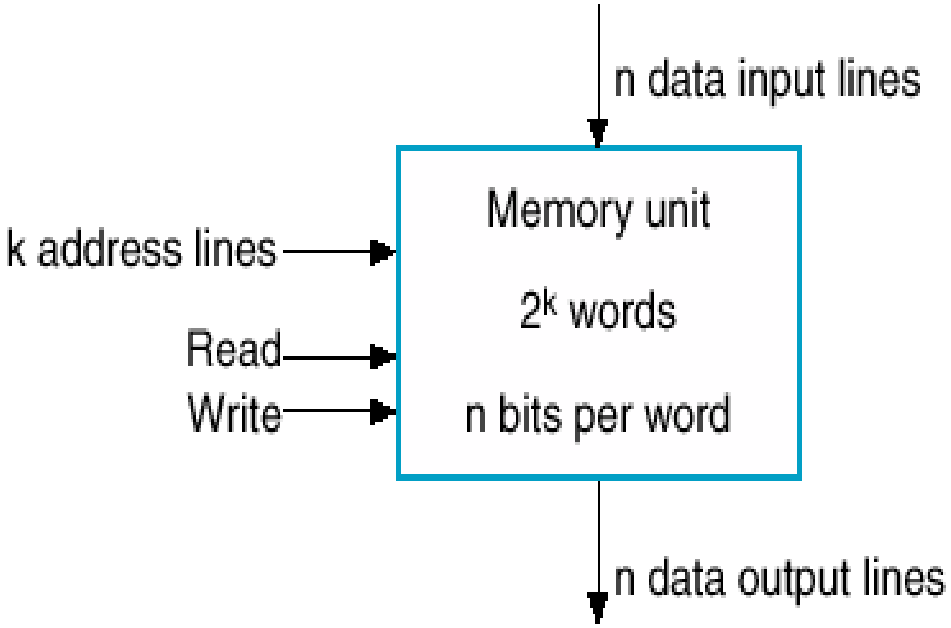
- Example cell: SRAM



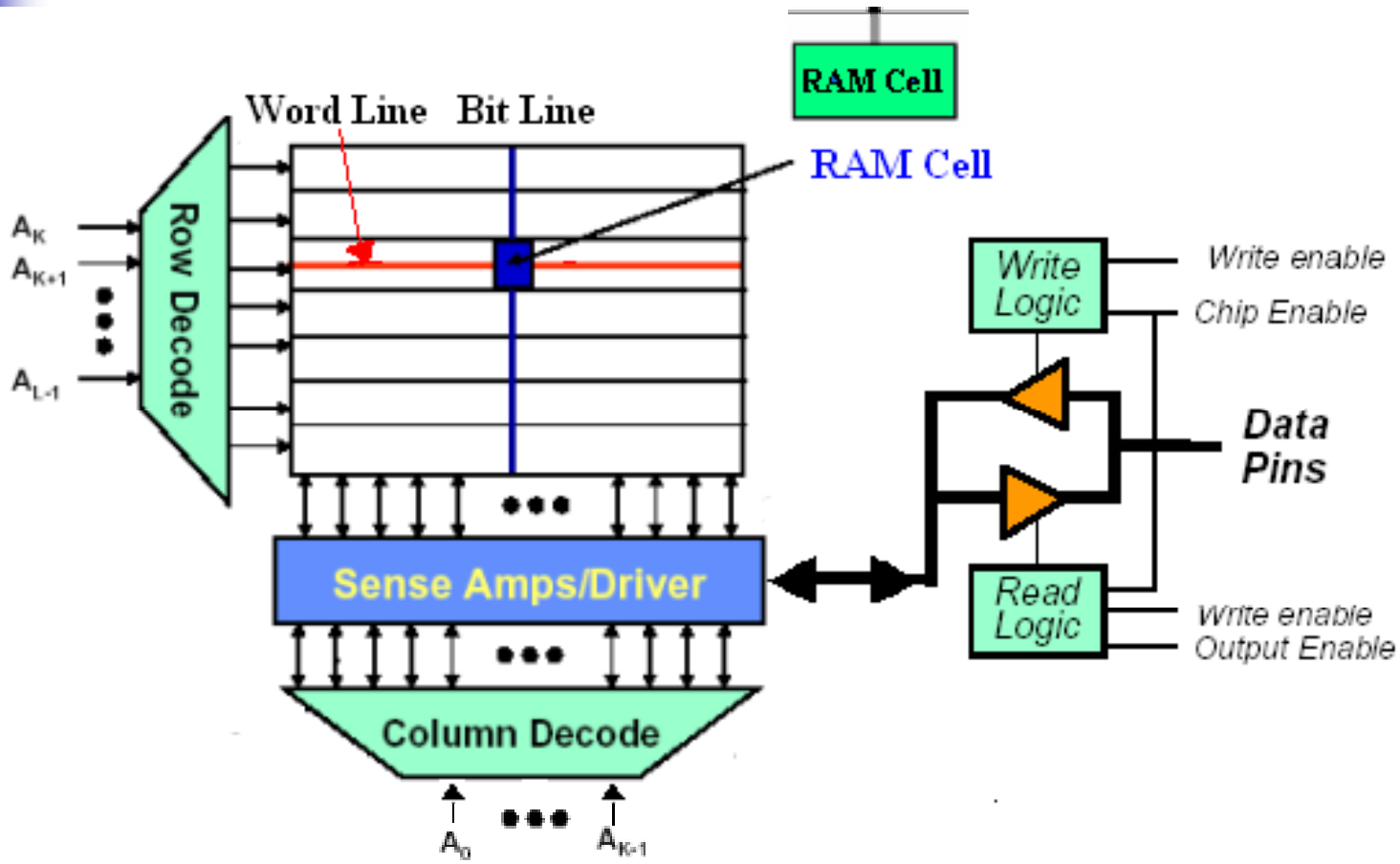
Simple View of RAM

- **RAM Naming Convention**

  - Examples: 32 X 8, "32 by 8" => 32 8-bit words



RAM Architecture

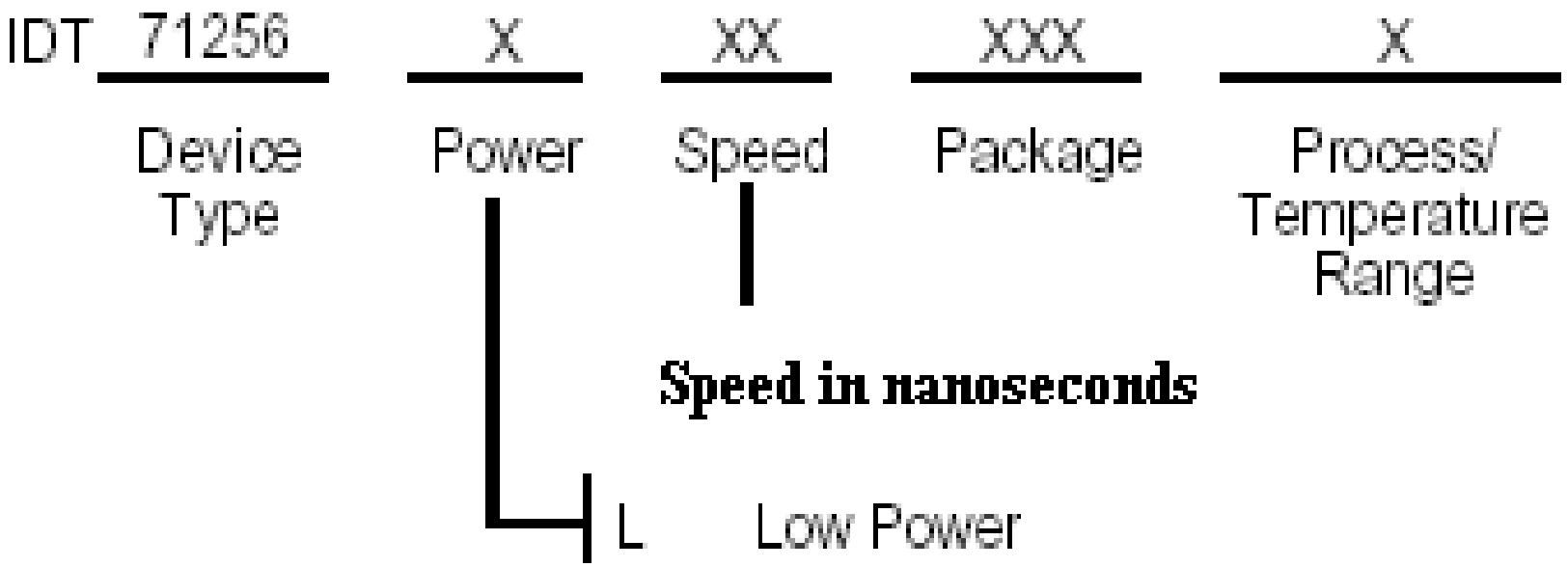


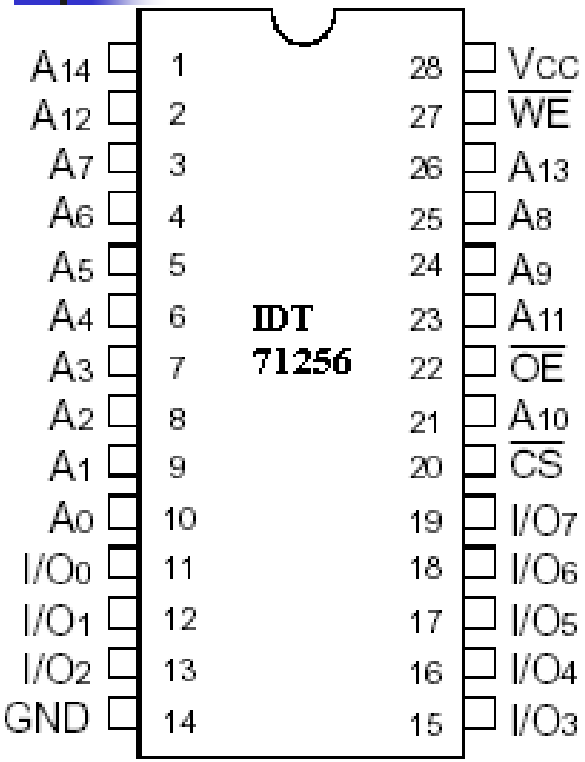
1K x 16 memory

- 10 address lines and 16 data lines

Memory address		Memory contents
Binary	Decimal	
0000000000	0	10110101 01011100
0000000001	1	10101011 10001001
0000000010	2	00001101 01000110
	⋮	⋮
1111111101	1021	10011101 00010101
1111111110	1022	00001101 00011110
1111111111	1023	11011110 00100100

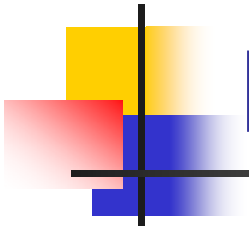
IDT Static RAM





Truth Table

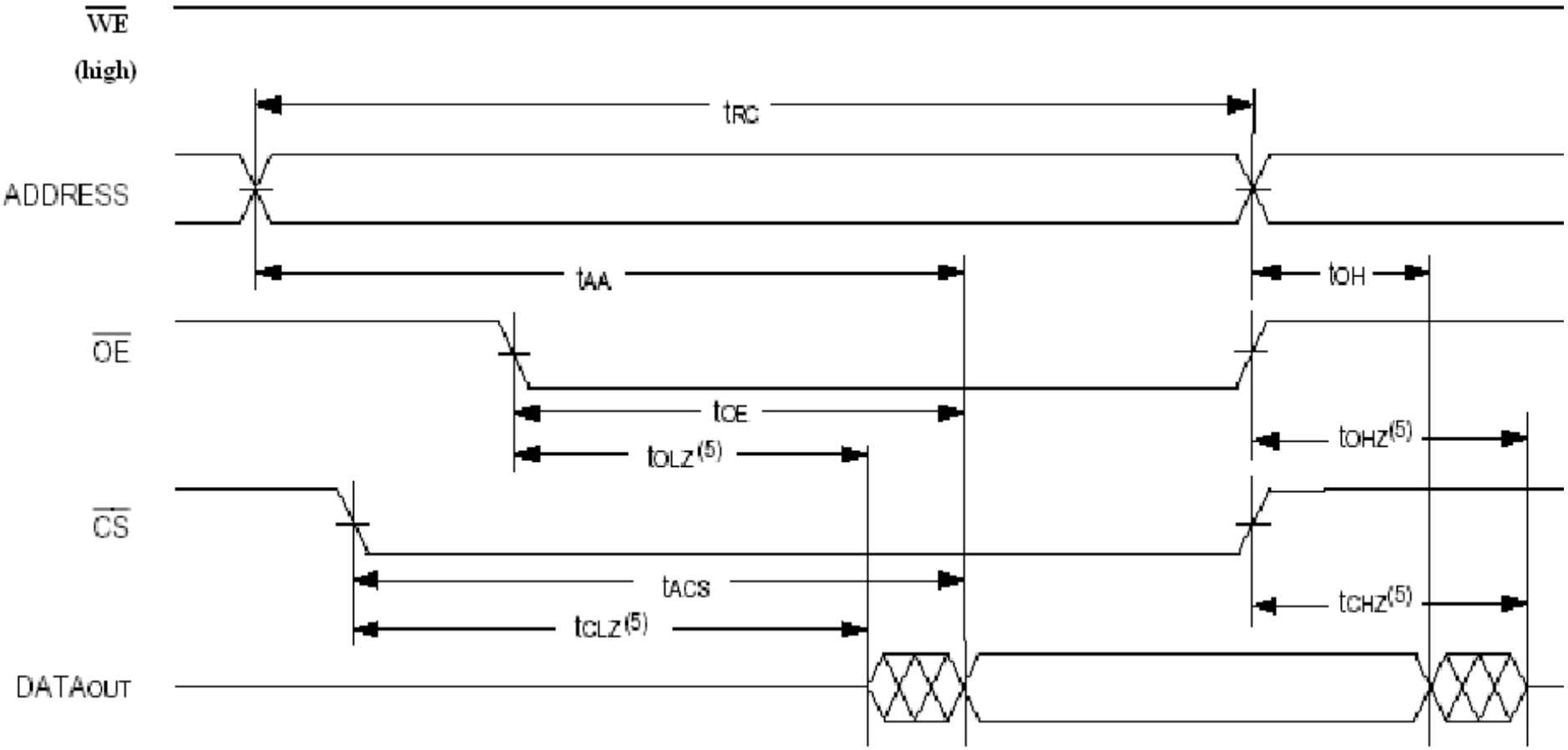
$\overline{WE}$	$\overline{CS}$	$\overline{OE}$	I/O	Function
X	H	X	High-Z	Standby
H	L	H	High-Z	Output Disabled
H	L	L	DOUT	Read Data
L	L	X	DIN	Write Data



Reading

- Steps
  - Setup address lines
  - Activate read line
  - Data available *after specified amount of time*

Read Cycle

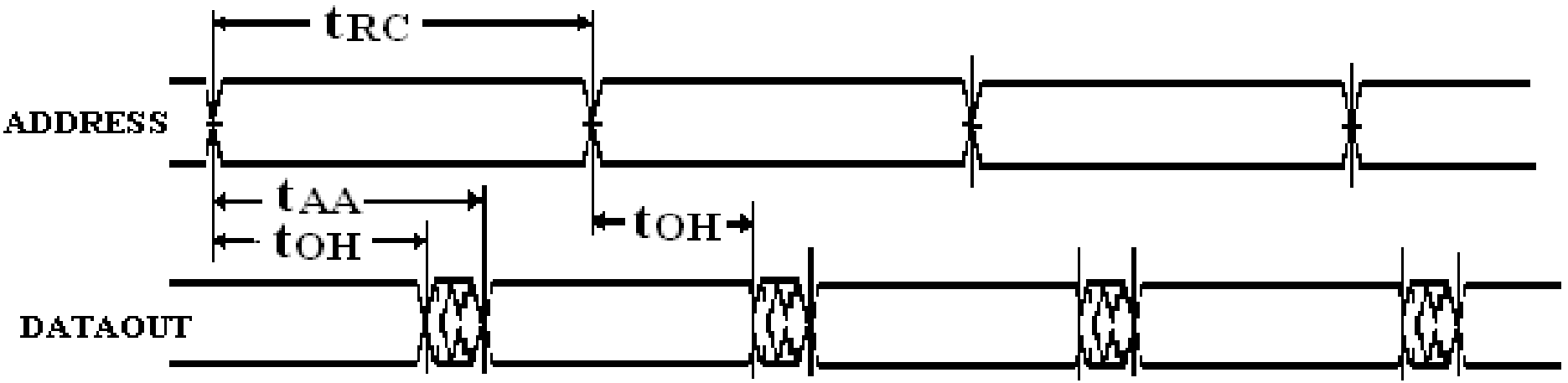

WE
(high)
ADDRESS
OE
CS
DATAOUT
tRC
tAA
tOH
tOE
tOLZ(5)
tOHZ(5)
tACS
tCLZ(5)
tCHZ(5)

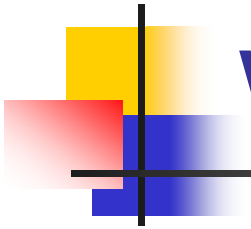
Read Cycle

Symbol	Parameter (ns)	71256S55 71256L55		71256S70 71256L70		71256S85 71256L85		71256S100 71256L100	
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
t_{RC}	Read Cycle Time	55	—	70	—	85	—	100	—
t_{AA}	Address Access Time	—	55	—	70	—	85	—	100
t_{ACS}	Chip Select Access Time	—	55	—	70	—	85	—	100
t_{CLZ}	Chip Select Time	5	—	5	—	5	—	5	—
t_{OE}	Output Enable to Output Valid	—	25	—	30	—	35	—	40
t_{OLZ}	Output Enable Time	0	—	0	—	0	—	0	—
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—

Multiple Read

$\overline{WE}$='1', $\overline{CS}$='0', $\overline{OE}$='0'

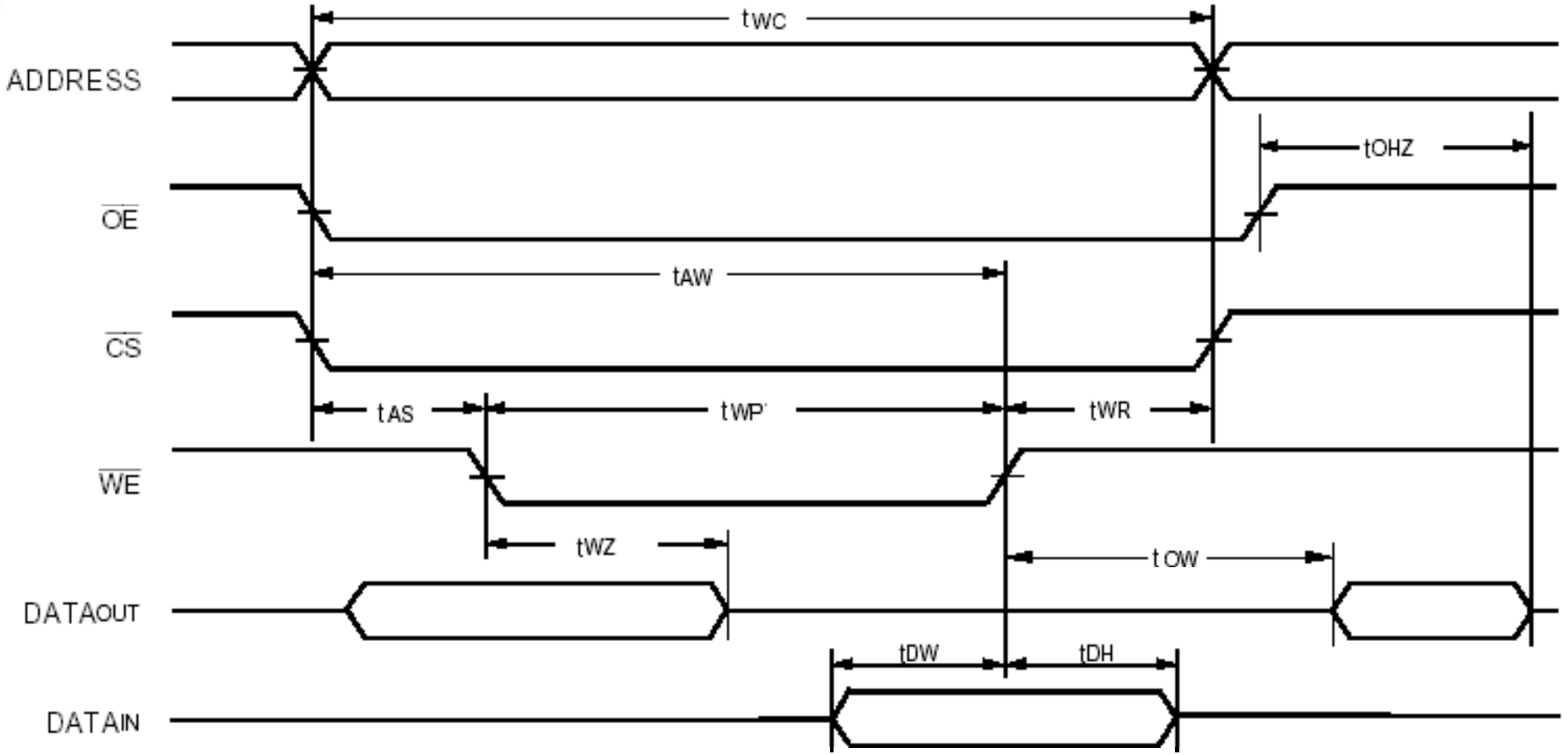




Writing

- Sequence of steps
  - Setup address lines
  - Setup data lines
  - Activate write line

Write Cycle


tWC
ADDRESS
tOHZ
OE
tAW
CS
tAS
tWP
tWR
WE
tWZ
tOW
DATAOUT
tDW
tDH
DATAIN

Write Cycle

Symbol	Parameter (ns)	71256S55 71256L55		71256S70 71256L70		71256S85 71256L85		71256S100 71256L100	
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
t_{WC}	Write Cycle Time	55	—	70	—	85	—	100	—
t_{AS}	Address Setup Time	0	—	0	—	0	—	0	—
t_{WP}	Write Pulse Width	40	—	45	—	50	—	55	—
t_{WR}	Address Hold Time	0	—	0	—	0	—	0	—
t_{DW}	Data Setup Time	25	—	30	—	35	—	40	—
t_{DH}	Data Hold from Write Time ($\overline{WE}$)	0	—	0	—	0	—	0	—