Character 16x2 LCD

CPE166  Advance Logic Design
Overview

- 4-bit data interface for compatibility with other Xilinx boards
- LCD_E, LCD_RS, LCD_RW
- 2 line x 16 character Display
- Each character location consist of 5 dot x 8 bit display
## Interface Signals

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>FPGA Pin</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>SF_D&lt;11&gt;</td>
<td>M15</td>
<td>Data bit DB7</td>
</tr>
<tr>
<td>SF_D&lt;10&gt;</td>
<td>P17</td>
<td>Data bit DB6</td>
</tr>
<tr>
<td>SF_D&lt;9&gt;</td>
<td>R16</td>
<td>Data bit DB5</td>
</tr>
<tr>
<td>SF_D&lt;8&gt;</td>
<td>R15</td>
<td>Data bit DB4</td>
</tr>
<tr>
<td>LCD_E</td>
<td>M18</td>
<td>Read/Write Enable Pulse</td>
</tr>
<tr>
<td>LCD_RS</td>
<td>L18</td>
<td>Register Select</td>
</tr>
<tr>
<td>LCD_RW</td>
<td>L17</td>
<td>Read/Write Control</td>
</tr>
</tbody>
</table>

- **Shared with StrataFlash pins SF_D<11:8>**
- 0: Disabled
- 1: Read/Write operation enabled
- 0: Instruction register during write operations. Busy Flash during read operations
- 1: Data for read or write operations
- 0: WRITE, LCD accepts data
- 1: READ, LCD presents data
Operation

- LCD uses 4-bit interface
- Data = 8 bit
- Upper nibble is transferred first, followed by lower nibble

Timings:
- LCD_RW, LCD_RS and Data must be set 40 ns before asserting of LCD_E
- LCD_RW, LCD_RS and Data must be hold 10 ns after de-asserting LCD_E
- 1 usec time between transfer of upper and lower nibble
- 40 usec time between transfer of two 8-bit data
Memory Map

It consist of:
1) DD RAM
2) CG ROM
3) CG RAM

1) DD RAM : Display Data RAM

- Stores the character code for each character of LCD Display
- Extra locations are used during shifting operations
Memory Map

2) CG ROM : Character Generator ROM

- Contains font bitmap for predefined characters that LCD can display
- Character code in DD RAM equates to a location in CG ROM
  
  e.g. 48H location refers to character ‘H’ (also 48 is ASCII value of H)
- Contains English ASCII characters and Japanese Characters

3) CG RAM : Character Generator RAM

- Provides space for 8 custom characters
# Command Set

<table>
<thead>
<tr>
<th>Function</th>
<th>LCD_RS</th>
<th>LCD_RW</th>
<th>DB7</th>
<th>DB6</th>
<th>DB5</th>
<th>DB4</th>
<th>DB3</th>
<th>DB2</th>
<th>DB1</th>
<th>DB0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clear Display</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>Return Cursor Home</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>-</td>
</tr>
<tr>
<td>Entry Mode Set</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>I/D</td>
<td>S</td>
</tr>
<tr>
<td>Display ON/OFF</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>D</td>
<td>C</td>
<td>B</td>
</tr>
<tr>
<td>Cursor and Display Shift</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>S/C</td>
<td>R/L</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Function Set</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Set CG RAM Address</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>A5</td>
<td>A4</td>
<td>A3</td>
<td>A2</td>
<td>A1</td>
<td>A0</td>
</tr>
<tr>
<td>Set DD RAM Address</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>A6</td>
<td>A5</td>
<td>A4</td>
<td>A3</td>
<td>A2</td>
<td>A1</td>
<td>A0</td>
</tr>
<tr>
<td>Read Busy Flag and Address</td>
<td>0</td>
<td>1</td>
<td>BF</td>
<td>A6</td>
<td>A5</td>
<td>A4</td>
<td>A3</td>
<td>A2</td>
<td>A1</td>
<td>A0</td>
</tr>
<tr>
<td>Write Data to CG RAM/DD RAM</td>
<td>1</td>
<td>0</td>
<td>D7</td>
<td>D6</td>
<td>D5</td>
<td>D4</td>
<td>D3</td>
<td>D2</td>
<td>D1</td>
<td>D0</td>
</tr>
<tr>
<td>Read from CG RAM/DD RAM</td>
<td>1</td>
<td>1</td>
<td>D7</td>
<td>D6</td>
<td>D5</td>
<td>D4</td>
<td>D3</td>
<td>D2</td>
<td>D1</td>
<td>D0</td>
</tr>
</tbody>
</table>
Command Set

• Disabled: LCD_E = 0 => All other inputs are ignored

• Clear Display:
  – Clears the Display
  – Returns cursor to top-left position
  – Writes a blank space to all DD RAM Location
  – Address counter is reset to 0
  – Clears all optional setting

• Return Cursor Home:
  – Returns cursor to top-left position
  – DD RAM content remains unchanged
  – Address counter is reset to 0
  – Display is returned to original status, if shifted
Command Set

• Entry Mode Set
  – Set cursor move direction
  – Specify whether or not to shift the display

Bit DB1 – I/D (Increment/Decrement)
0 - Auto Increment the address counter. Cursor blink/move to left
1 - Auto Decrement the address counter. Cursor blink/move to right

Bit DB0 – Shift
0 – Shifting Disabled
1 – During a DD RAM write operation, shift the entire display value in the direction controlled by Bit DB1 (I/D). Appears as though the cursor position remains constant and the display moves
Command Set

- Display ON/OFF: Display is turned on/off
  
  Bit DB2 (D) Display on/off
  0 – No character displayed. Data stored in DD RAM is retained
  1 – Display character stored in DD RAM

  Bit DB1 (C) Cursor on/off
  0 – No cursor
  1 – Display cursor

  Bit DB0 (B) Cursor blink on/off
  0 – No cursor blinking
  1 – Cursor blinks on/off approx. every half second
Command Set

- **Cursor and Display Shift:** Moves cursor and shifts display without changing the DD RAM contents

<table>
<thead>
<tr>
<th>DB3 (S/C)</th>
<th>DB2 (R/L)</th>
<th>Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Shift cursor left. Add. Counter decrement by 1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Shift cursor right. Add. Counter increment by 1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Shift entire display to left. Add. Counter remains unchanged</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Shift entire display to the right. Add. Counter remains unchanged</td>
</tr>
</tbody>
</table>
Command Set

- Function Set:
  - Sets interface data length
  - Number of display lines
  - Character font
  - Starter kit – Value = 28h

- Set CG RAM Address:
  - Sets initial CG RAM Address
  - Subsequent data read/write is performed from CG RAM

- Set DD RAM Address:
  - Sets initial DD RAM Address
  - Subsequent data read/write is performed from DD RAM

- Read Busy Flag and Address:
  - BF = 1 => Some internal operation is in progress. Next instruction is not accepted until the flag clears
  - Returns present value of the Address Counter
Command Set

- **Write Data to CG RAM or DD RAM:**
  - Writes data to CG RAM / DDRAM if followed by Set CG RAM / DD RAM Address respectively
  - Add. Counter automatically inc. or dec. depending upon I/D bit

- **Read Data from CG RAM or DD RAM:**
  - Reads data from CG RAM / DDRAM if followed by Set CG RAM / DD RAM Address respectively
  - Add. Counter automatically inc. or dec. depending upon I/D bit
Initializing Display

• Power-On Initialization:
  – Wait 15 msec, write SF_D<11:8> = 03h, for 12 clock
  – Wait 4.1 msec, write SF_D<11:8> = 03h, for 12 clock
  – Wait 100 usec, write SF_D<11:8> = 03h, for 12 clock
  – Wait 40 usec, write SF_D<11:8> = 02h, for 12 clock
  – Wait 20 usec
  – Timings are as per the given specs for this LCD

• Display Configuration:
  – Function Set
  – Entry Mode set
  – Display On/Off
  – Clear Display
  – Write data to Display
  – Disable unused LCD (LCD_E = low, LCD_RW = low)
References

• Spartan 3E Starter Kit User Guide, UG230 (V 1.0), March 9 ’06