Character LCD Screen

Overview

The Spartan-3E Starter Kit board prominently features a 2-line by 16-character liquid crystal display (LCD). The FPGA controls the LCD via the 4-bit data interface shown in Figure 5-1. Although the LCD supports an 8-bit data interface, the Starter Kit board uses a 4-bit data interface to remain compatible with other Xilinx development boards and to minimize total pin count.

Once mastered, the LCD is a practical way to display a variety of information using standard ASCII and custom characters. However, these displays are not fast. Scrolling the display at half-second intervals tests the practical limit for clarity. Compared with the 50 MHz clock available on the board, the display is slow. A PicoBlaze processor efficiently controls display timing plus the actual content of the display.
Chapter 5: Character LCD Screen

Character LCD Interface Signals

Table 5-1 shows the interface character LCD interface signals.

Table 5-1: Character LCD Interface

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>FPGA Pin</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>SF_D&lt;11&gt;</td>
<td>M15</td>
<td>Data bit DB7 Shared with StrataFlash pins SF_D&lt;11:8&gt;</td>
</tr>
<tr>
<td>SF_D&lt;10&gt;</td>
<td>P17</td>
<td>Data bit DB6</td>
</tr>
<tr>
<td>SF_D&lt;9&gt;</td>
<td>R16</td>
<td>Data bit DB5</td>
</tr>
<tr>
<td>SF_D&lt;8&gt;</td>
<td>R15</td>
<td>Data bit DB4</td>
</tr>
<tr>
<td>LCD_E</td>
<td>M18</td>
<td>Read/Write Enable Pulse 0: Disabled 1: Read/Write operation enabled</td>
</tr>
<tr>
<td>LCD_RS</td>
<td>L18</td>
<td>Register Select 0: Instruction register during write operations. Busy Flash during read operations 1: Data for read or write operations</td>
</tr>
<tr>
<td>LCD_RW</td>
<td>L17</td>
<td>Read/Write Control 0: WRITE, LCD accepts data 1: READ, LCD presents data</td>
</tr>
</tbody>
</table>

Voltage Compatibility

The character LCD is powered by +5V. The FPGA I/O signals are powered by 3.3V. However, the FPGA’s output levels are recognized as valid Low or High logic levels by the LCD. The LCD controller accepts 5V TTL signal levels and the 3.3V LVCMOS outputs provided by the FPGA meet the 5V TTL voltage level requirements.

The 390Ω series resistors on the data lines prevent overstressing on the FPGA and StrataFlash I/O pins when the character LCD drives a High logic value. The character LCD drives the data lines when LCD_RW is High. Most applications treat the LCD as a write-only peripheral and never read from the display.

Interaction with Intel StrataFlash

As shown in Figure 5-1, the four LCD data signals are also shared with StrataFlash data lines SF_D<11:8>. As shown in Table 5-2, the LCD/StrataFlash interaction depends on the application usage in the design. When the StrataFlash memory is disabled (SF_CE0 = High), then the FPGA application has full read/write access to the LCD. Conversely, when LCD read operations are disabled (LCD_RW = Low), then the FPGA application has full read/write access to the StrataFlash memory.

Table 5-2: LCD/StrataFlash Control Interaction

<table>
<thead>
<tr>
<th>SF_CE0</th>
<th>SF_BYTE</th>
<th>LCD_RW</th>
<th>Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>X</td>
<td>X</td>
<td>StrataFlash disabled. Full read/write access to LCD.</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
<td>0</td>
<td>LCD write access only. Full access to StrataFlash.</td>
</tr>
<tr>
<td>X</td>
<td>0</td>
<td>X</td>
<td>StrataFlash in byte-wide (x8) mode. Upper data lines are not used. Full access to both LCD and StrataFlash.</td>
</tr>
</tbody>
</table>

Notes:
1. ‘X’ indicates a don’t care, can be either 0 or 1.
If the StrataFlash memory is in byte-wide (x8) mode (SF_BYTE = Low), the FPGA application has full simultaneous read/write access to both the LCD and the StrataFlash memory. In byte-wide mode, the StrataFlash memory does not use the SF_D<15:8> data lines.

UCF Location Constraints

Figure 5-2 provides the UCF constraints for the Character LCD, including the I/O pin assignment and the I/O standard used.

```
NET "LCD_E" LOC = "M18" | IOSTANDARD = LVCMOS33 | DRIVE = 4 | SLEW = SLOW ;
NET "LCD_RS" LOC = "L18" | IOSTANDARD = LVCMOS33 | DRIVE = 4 | SLEW = SLOW ;
NET "LCD_RW" LOC = "L17" | IOSTANDARD = LVCMOS33 | DRIVE = 4 | SLEW = SLOW ;

# The LCD four-bit data interface is shared with the StrataFlash.
NET "SF_D<8>" LOC = "R15" | IOSTANDARD = LVCMOS33 | DRIVE = 4 | SLEW = SLOW ;
NET "SF_D<9>" LOC = "R16" | IOSTANDARD = LVCMOS33 | DRIVE = 4 | SLEW = SLOW ;
NET "SF_D<10>" LOC = "P17" | IOSTANDARD = LVCMOS33 | DRIVE = 4 | SLEW = SLOW ;
NET "SF_D<11>" LOC = "M15" | IOSTANDARD = LVCMOS33 | DRIVE = 4 | SLEW = SLOW ;
```

Figure 5-2: UCF Location Constraints for the Character LCD

LCD Controller

The 2 x 16 character LCD has an internal Sitronix ST7066U graphics controller that is functionally equivalent with the following devices.

- Samsung S6A0069X or KS0066U
- Hitachi HD44780
- SMOS SED1278

Memory Map

The controller has three internal memory regions, each with a specific purpose. The display must be initialized before accessing any of these memory regions.

DD RAM

The Display Data RAM (DD RAM) stores the character code to be displayed on the screen. Most applications interact primarily with DD RAM. The character code stored in a DD RAM location references a specific character bitmap stored either in the predefined CG ROM character set or in the user-defined CG RAM character set.

Figure 5-3 shows the default address for the 32 character locations on the display. The upper line of characters is stored between addresses 0x00 and 0x0F. The second line of characters is stored between addresses 0x40 and 0x4F.

```
Character Display Addresses
00 01 02 03 04 05 06 07 08 09 0A 0B 0C 0D 0E 0F
40 41 42 43 44 45 46 47 48 49 4A 4B 4C 4D 4E 4F
```

Figure 5-3: DD RAM Hexadecimal Addresses (No Display Shifting)
Physically, there are 80 total character locations in DD RAM with 40 characters available per line. Locations 0x10 through 0x27 and 0x50 through 0x67 can be used to store other non-display data. Alternatively, these locations can also store characters that can only displayed using controller’s display shifting functions.

The Set DD RAM Address command initializes the address counter before reading or writing to DD RAM. Write DD RAM data using the Write Data to CG RAM or DD RAM command, and read DD RAM using the Read Data from CG RAM or DD RAM command.

The DD RAM address counter either remains constant after read or write operations, or auto-increments or auto-decrements by one location, as defined by the I/D set by the Entry Mode Set command.

**CG ROM**

The Character Generator ROM (CG ROM) contains the font bitmap for each of the predefined characters that the LCD screen can display, shown in Figure 5-4. The character code stored in DD RAM for each character location subsequently references a position with the CG ROM. For example, a hexadecimal character code of 0x53 stored in a DD RAM location displays the character ‘S’. The upper nibble of 0x53 equates to DB[7:4] = "0101" binary and the lower nibble equates to DB[3:0] = “0011” binary. As shown in Figure 5-4, the character ‘S’ appears on the screen.

English/Roman characters are stored in CG ROM at their equivalent ASCII code address.
The character ROM contains the ASCII English character set and Japanese kana characters. The controller also provides for eight custom character bitmaps, stored in CG RAM. These eight custom characters are displayed by storing character codes 0x00 through 0x07 in a DD RAM location.

**CG RAM**

The Character Generator RAM (CG RAM) provides space to create eight custom character bitmaps. Each custom character location consists of a 5-dot by 8-line bitmap, as shown in Figure 5-5.

The Set CG RAM Address command initializes the address counter before reading or writing to CG RAM. Write CG RAM data using the Write Data to CG RAM or DD RAM command, and read CG RAM using the Read Data from CG RAM or DD RAM command.
The CG RAM address counter can either remain constant after read or write operations, or auto-increments or auto-decrements by one location, as defined by the I/D set by the Entry Mode Set command.

Figure 5-5 provides an example, creating a special checkerboard character. The custom character is stored in the fourth CG RAM character location, which is displayed when a DD RAM location is 0x03. To write the custom character, the CG RAM address is first initialized using the Set CG RAM Address command. The upper three address bits point to the custom character location. The lower three address bits point to the row address for the character bitmap. The Write Data to CG RAM or DD RAM command is used to write each character bitmap row. A ‘1’ lights a bit on the display. A ‘0’ leaves the bit unlit. Only the lower five data bits are used; the upper three data bits are don’t care positions. The eighth row of bitmap data is usually left as all zeros to accommodate the cursor.

<table>
<thead>
<tr>
<th>Character Address</th>
<th>Row Address</th>
<th>Don’t Care</th>
<th>Character Bitmap</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 1 1 0 0 0 0 0</td>
<td>- - -</td>
<td>0 0 0 0 0</td>
<td></td>
</tr>
<tr>
<td>0 1 1 0 0 1 1 1</td>
<td>- - -</td>
<td>0 0 0 0 0</td>
<td></td>
</tr>
<tr>
<td>0 1 1 0 1 0 0 0</td>
<td>- - -</td>
<td>0 0 0 0 0</td>
<td></td>
</tr>
<tr>
<td>0 1 1 0 1 1 1 1</td>
<td>- - -</td>
<td>0 0 0 0 0</td>
<td></td>
</tr>
<tr>
<td>0 1 1 1 0 0 0 0</td>
<td>- - -</td>
<td>0 0 0 0 0</td>
<td></td>
</tr>
<tr>
<td>0 1 1 1 1 0 1 1</td>
<td>- - -</td>
<td>0 0 0 0 0</td>
<td></td>
</tr>
<tr>
<td>0 1 1 1 1 1 0 0</td>
<td>- - -</td>
<td>0 0 0 0 0</td>
<td></td>
</tr>
<tr>
<td>0 1 1 1 1 1 1 1</td>
<td>- - -</td>
<td>0 0 0 0 0</td>
<td></td>
</tr>
</tbody>
</table>

*Figure 5-5: Example Custom Checkerboard Character with Character Code 0x03*

**Command Set**

Table 5-3 summarizes the available LCD controller commands and bit definitions. Because the display is set up for 4-bit operation, each 8-bit command is sent as two 4-bit nibbles. The upper nibble is transferred first, followed by the lower nibble.

<table>
<thead>
<tr>
<th>Function</th>
<th>LCD_RS</th>
<th>LCD_RW</th>
<th>Upper Nibble</th>
<th>Lower Nibble</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clear Display</td>
<td>0 0</td>
<td>0</td>
<td>0 0 0 0 0</td>
<td>0 0 0 0 0</td>
</tr>
<tr>
<td>Return Cursor Home</td>
<td>0 0</td>
<td>0</td>
<td>0 0 0 0 0</td>
<td>0 0 0 0 0</td>
</tr>
<tr>
<td>Entry Mode Set</td>
<td>0 0</td>
<td>0</td>
<td>0 0 0 0 0</td>
<td>0 1 1 D C B</td>
</tr>
<tr>
<td>Display On/Off</td>
<td>0 0</td>
<td>0</td>
<td>0 0 0 0 0</td>
<td>1 S/C R/L -</td>
</tr>
<tr>
<td>Cursor and Display Shift</td>
<td>0 0</td>
<td>0</td>
<td>0 0 0 0 1</td>
<td>S/C R/L -  -</td>
</tr>
</tbody>
</table>

*Table 5-3: LCD Character Display Command Set*
Table 5-3: LCD Character Display Command Set (Continued)

<table>
<thead>
<tr>
<th>Function</th>
<th>LCD_RS</th>
<th>LCD_RW</th>
<th>UpperNibble</th>
<th>LowerNibble</th>
</tr>
</thead>
<tbody>
<tr>
<td>Function Set</td>
<td>0</td>
<td>0</td>
<td>0 0 1 0</td>
<td>1 0 - -</td>
</tr>
<tr>
<td>Set CG RAM Address</td>
<td>0</td>
<td>0</td>
<td>0 1 A5 A4</td>
<td>A3 A2 A1 A0</td>
</tr>
<tr>
<td>Set DD RAM Address</td>
<td>0</td>
<td>1</td>
<td>1 A6 A5 A4</td>
<td>A3 A2 A1 A0</td>
</tr>
<tr>
<td>Read Busy Flag and Address</td>
<td>0</td>
<td>1</td>
<td>BF A6 A5 A4</td>
<td>A3 A2 A1 A0</td>
</tr>
<tr>
<td>Write Data to CG RAM or DD RAM</td>
<td>1</td>
<td>0</td>
<td>D7 D6 D5 D4</td>
<td>D3 D2 D1 D0</td>
</tr>
<tr>
<td>Read Data from CG RAM or DD RAM</td>
<td>1</td>
<td>1</td>
<td>D7 D6 D5 D4</td>
<td>D3 D2 D1 D0</td>
</tr>
</tbody>
</table>

Disabled

If the LCD_E enable signal is Low, all other inputs to the LCD are ignored.

Clear Display

Clear the display and return the cursor to the home position, the top-left corner.

This command writes a blank space (ASCII/ANSI character code 0x20) into all DD RAM addresses. The address counter is reset to 0, location 0x00 in DD RAM. Clears all option settings. The I/D control bit is set to 1 (increment address counter mode) in the Entry Mode Set command.

Execution Time: 82 μs – 1.64 ms

Return Cursor Home

Return the cursor to the home position, the top-left corner. DD RAM contents are unaffected. Also returns the display being shifted to the original position, shown in Figure 5-3.

The address counter is reset to 0, location 0x00 in DD RAM. The display is returned to its original status if it was shifted. The cursor or blink move to the top-left character location.

Execution Time: 40 μs – 1.6 ms

Entry Mode Set

Sets the cursor move direction and specifies whether or not to shift the display.

These operations are performed during data reads and writes.

Execution Time: 40 μs

Bit DB1: (I/D) Increment/Decrement

<table>
<thead>
<tr>
<th></th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Auto-decrement address counter. Cursor/blink moves to left.</td>
</tr>
<tr>
<td>1</td>
<td>Auto-increment address counter. Cursor/blink moves to right.</td>
</tr>
</tbody>
</table>
This bit either auto-increments or auto-decrements the DD RAM and CG RAM address counter by one location after each Write Data to CG RAM or DD RAM or Read Data from CG RAM or DD RAM command. The cursor or blink position moves accordingly.

**Bit DB0: (S) Shift**

<table>
<thead>
<tr>
<th>0</th>
<th>Shifting disabled</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>During a DD RAM write operation, shift the entire display value in the direction controlled by Bit DB1 (I/D). Appears as though the cursor position remains constant and the display moves.</td>
</tr>
</tbody>
</table>

**Display On/Off**

Display is turned on or off, controlling all characters, cursor and cursor position character (underscore) blink.

Execution Time: 40 μs

**Bit DB2: (D) Display On/Off**

<table>
<thead>
<tr>
<th>0</th>
<th>No characters displayed. However, data stored in DD RAM is retained</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Display characters stored in DD RAM</td>
</tr>
</tbody>
</table>

**Bit DB1: (C) Cursor On/Off**

The cursor uses the five dots on the bottom line of the character. The cursor appears as a line under the displayed character.

<table>
<thead>
<tr>
<th>0</th>
<th>No cursor</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Display cursor</td>
</tr>
</tbody>
</table>

**Bit DB0: (B) Cursor Blink On/Off**

<table>
<thead>
<tr>
<th>0</th>
<th>No cursor blinking</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Cursor blinks on and off approximately every half second</td>
</tr>
</tbody>
</table>

**Cursor and Display Shift**

Moves the cursor and shifts the display without changing DD RAM contents. Shift cursor position or display to the right or left without writing or reading display data.

This function positions the cursor in order to modify an individual character, or to scroll the display window left or right to reveal additional data stored in the DD RAM, beyond the 16th character on a line. The cursor automatically moves to the second line when it shifts beyond the 40th character location of the first line. The first and second line displays shift at the same time.

When the displayed data is shifted repeatedly, both lines move horizontally. The second display line does not shift into the first display line.

Execution Time: 40 μs
Table 5-4: Shift Patterns According to S/C and R/L Bits

<table>
<thead>
<tr>
<th>DB3 (S/C)</th>
<th>DB2 (R/L)</th>
<th>Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 0</td>
<td></td>
<td>Shift the cursor position to the left. The address counter is decremented</td>
</tr>
<tr>
<td>0 1</td>
<td></td>
<td>Shift the cursor position to the right. The address counter is incremented</td>
</tr>
<tr>
<td>1 0</td>
<td></td>
<td>Shift the entire display to the left. The cursor follows the display shift. The address counter is unchanged.</td>
</tr>
<tr>
<td>1 1</td>
<td></td>
<td>Shift the entire display to the right. The cursor follows the display shift. The address counter is unchanged.</td>
</tr>
</tbody>
</table>

Function Set

Sets interface data length, number of display lines, and character font.

The Starter Kit board supports a single function set with value 0x28.

Execution Time: 40 μs

Set CG RAM Address

Set the initial CG RAM address.

After this command, all subsequent read or write operations to the display are to or from CG RAM.

Execution Time: 40 μs

Set DD RAM Address

Set the initial DD RAM address.

After this command, all subsequent read or write operations to the display are to or from DD RAM. The addresses for displayed characters appear in Figure 5-3.

Execution Time: 40 μs

Read Busy Flag and Address

Read the Busy flag (BF) to determine if an internal operation is in progress, and read the current address counter contents.

BF = 1 indicates that an internal operation is in progress. The next instruction is not accepted until BF is cleared or until the current instruction is allowed the maximum time to execute.

This command also returns the present value of address counter. The address counter is used for both CG RAM and DD RAM addresses. The specific context depends on the most recent Set CG RAM Address or Set DD RAM Address command issued.

Execution Time: 1 μs

Write Data to CG RAM or DD RAM

Write data into DD RAM if the command follows a previous Set DD RAM Address command, or write data into CG RAM if the command follows a previous Set CG RAM Address command.
After the write operation, the address is automatically incremented or decremented by 1 according to the Entry Mode Set command. The entry mode also determines display shift.

Execution Time: 40 μs

Read Data from CG RAM or DD RAM

Read data from DD RAM if the command follows a previous Set DD RAM Address command, or read data from CG RAM if the command follows a previous Set CG RAM Address command.

After the read operation, the address is automatically incremented or decremented by 1 according to the Entry Mode Set command. However, a display shift is not executed during read operations.

Execution Time: 40 μs

Operation

Four-Bit Data Interface

The board uses a 4-bit data interface to the character LCD.

Figure 5-6 illustrates a write operation to the LCD, showing the minimum times allowed for setup, hold, and enable pulse length relative to the 50 MHz clock (20 ns period) provided on the board.

![Character LCD Interface Timing Diagram](image-url)
The data values on SF_D<11:8>, and the register select (LCD_RS) and the read/write (LCD_RW) control signals must be set up and stable at least 40 ns before the enable LCD_E goes High. The enable signal must remain High for 230 ns or longer—the equivalent of 12 or more clock cycles at 50 MHz.

In many applications, the LCD_RW signal can be tied Low permanently because the FPGA generally has no reason to read information from the display.

Transferring 8-Bit Data over the 4-Bit Interface

After initializing the display and establishing communication, all commands and data transfers to the character display are via 8 bits, transferred using two sequential 4-bit operations. Each 8-bit transfer must be decomposed into two 4-bit transfers, spaced apart by at least 1 μs, as shown in Figure 5-6. The upper nibble is transferred first, followed by the lower nibble. An 8-bit write operation must be spaced least 40 μs before the next communication. This delay must be increased to 1.64 ms following a Clear Display command.

Initializing the Display

After power-on, the display must be initialized to establish the required communication protocol. The initialization sequence is simple and ideally suited to the highly-efficient 8-bit PicoBlaze embedded controller. After initialization, the PicoBlaze controller is available for more complex control or computation beyond simply driving the display.

Power-On Initialization

The initialization sequence first establishes that the FPGA application wishes to use the four-bit data interface to the LCD as follows:

- Wait 15 ms or longer, although the display is generally ready when the FPGA finishes configuration. The 15 ms interval is 750,000 clock cycles at 50 MHz.
- Write SF_D<11:8> = 0x3, pulse LCD_E High for 12 clock cycles.
- Wait 4.1 ms or longer, which is 205,000 clock cycles at 50 MHz.
- Write SF_D<11:8> = 0x3, pulse LCD_E High for 12 clock cycles.
- Wait 100 μs or longer, which is 5,000 clock cycles at 50 MHz.
- Write SF_D<11:8> = 0x3, pulse LCD_E High for 12 clock cycles.
- Wait 40 μs or longer, which is 2,000 clock cycles at 50 MHz.
- Write SF_D<11:8> = 0x2, pulse LCD_E High for 12 clock cycles.
- Wait 40 μs or longer, which is 2,000 clock cycles at 50 MHz.

Display Configuration

After the power-on initialization is completed, the four-bit interface is now established. The next part of the sequence configures the display:

- Issue a Function Set command, 0x28, to configure the display for operation on the Spartan-3E Starter Kit board.
- Issue an Entry Mode Set command, 0x06, to set the display to automatically increment the address pointer.
- Issue a Display On/Off command, 0x0C, to turn the display on and disables the cursor and blinking.
Finally, issue a Clear Display command. Allow at least 1.64 ms (82,000 clock cycles) after issuing this command.

Writing Data to the Display

To write data to the display, specify the start address, followed by one or more data values. Before writing any data, issue a Set DD RAM Address command to specify the initial 7-bit address in the DD RAM. See Figure 5-3 for DD RAM locations.

Write data to the display using a Write Data to CG RAM or DD RAM command. The 8-bit data value represents the look-up address into the CG ROM or CG RAM, shown in Figure 5-4. The stored bitmap in the CG ROM or CG RAM drives the 5 x 8 dot matrix to represent the associated character.

If the address counter is configured to auto-increment, as described earlier, the application can sequentially write multiple character codes and each character is automatically stored and displayed in the next available location.

Continuing to write characters, however, eventually falls off the end of the first display line. The additional characters do not automatically appear on the second line because the DD RAM map is not consecutive from the first line to the second.

Disabling the Unused LCD

If the FPGA application does not use the character LCD screen, drive the LCD_E pin Low to disable it. Also drive the LCD_RW pin Low to prevent the LCD screen from presenting data.

Related Resources

- Initial Design for Spartan-3E Starter Kit (Reference Design)
  http://www.xilinx.com/s3estarter
- PowerTip PC1602-D Character LCD (Basic Electrical and Mechanical Data)
- Sitronix ST7066U Character LCD Controller
- Detailed Data Sheet on PowerTip Character LCD
  http://www.rapidelectronics.co.uk/images/siteimg/57-0910e.PDF
- Samsung S6A0069X Character LCD Controller
  http://www.samsung.com/Products/Semiconductor/DisplayDriverIC/MobileDDI/BWSTN/S6A0069X/S6A0069X.htm